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# H61M06

Fab A

Micro ATX 8.9X6.8

**CPU:**

Intel Sandy Bridge processors in LGA1155 Package

**System Chipset:**

PCH

**Main Memory:**

Dual Channel / DDR-III \* 2 (Max 8GB)

**On Board Device:**

SIO: IT8772

LAN: Realtek RTL8111F/8105E

HDA Codec: ALC662

BIOS:SPI Flash ROM 4Mbyte

**Expansion Slots:**

PCI EXPRESS 16X SLOT \*1


PCI EXPRESS 1X SLOT \* 2

H61MXE-S      USB3+RTL8111F+POWER MOS+Solid CAP

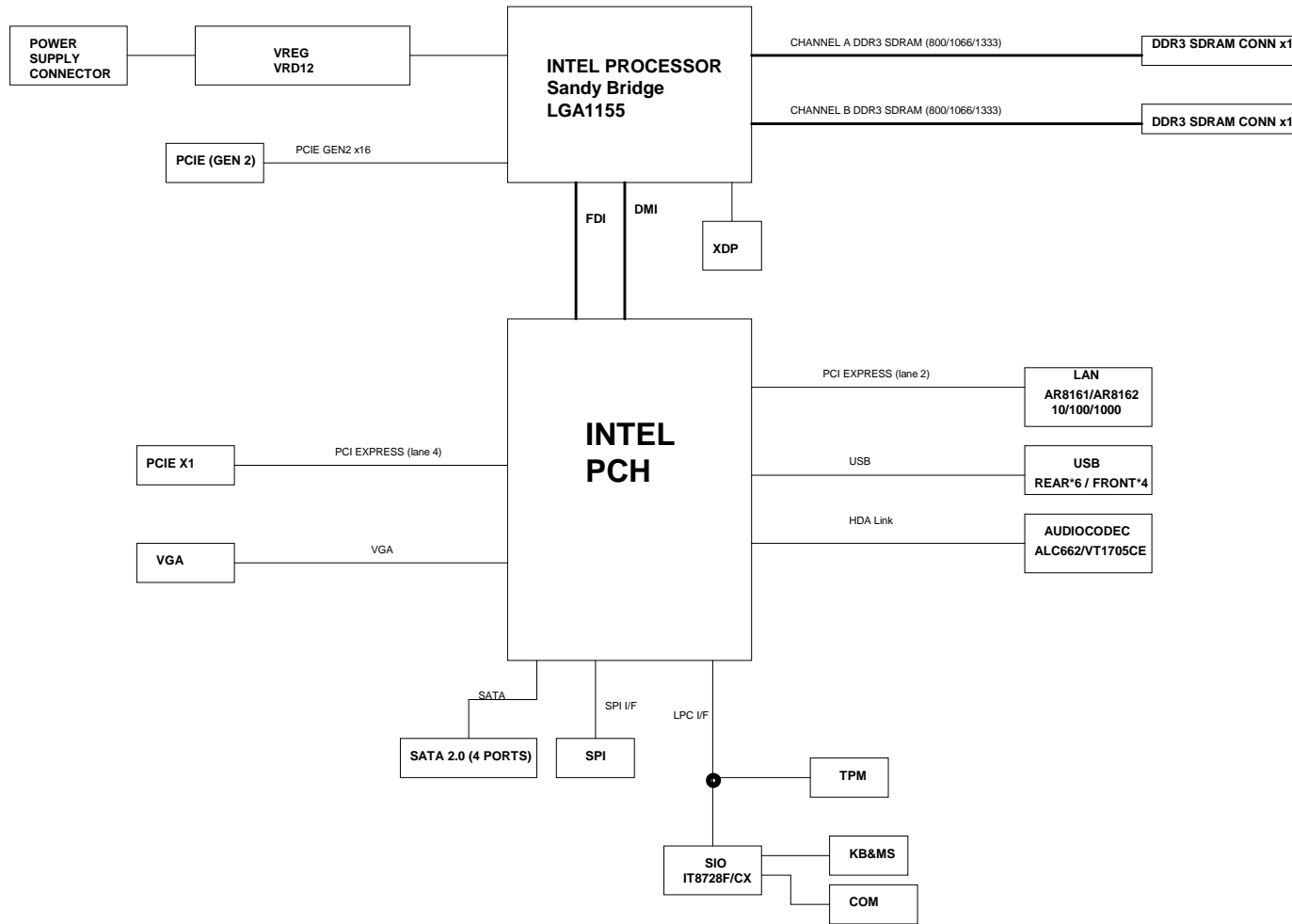
H61MXE      RTL8111F

H61MXE-V      RTL8105E

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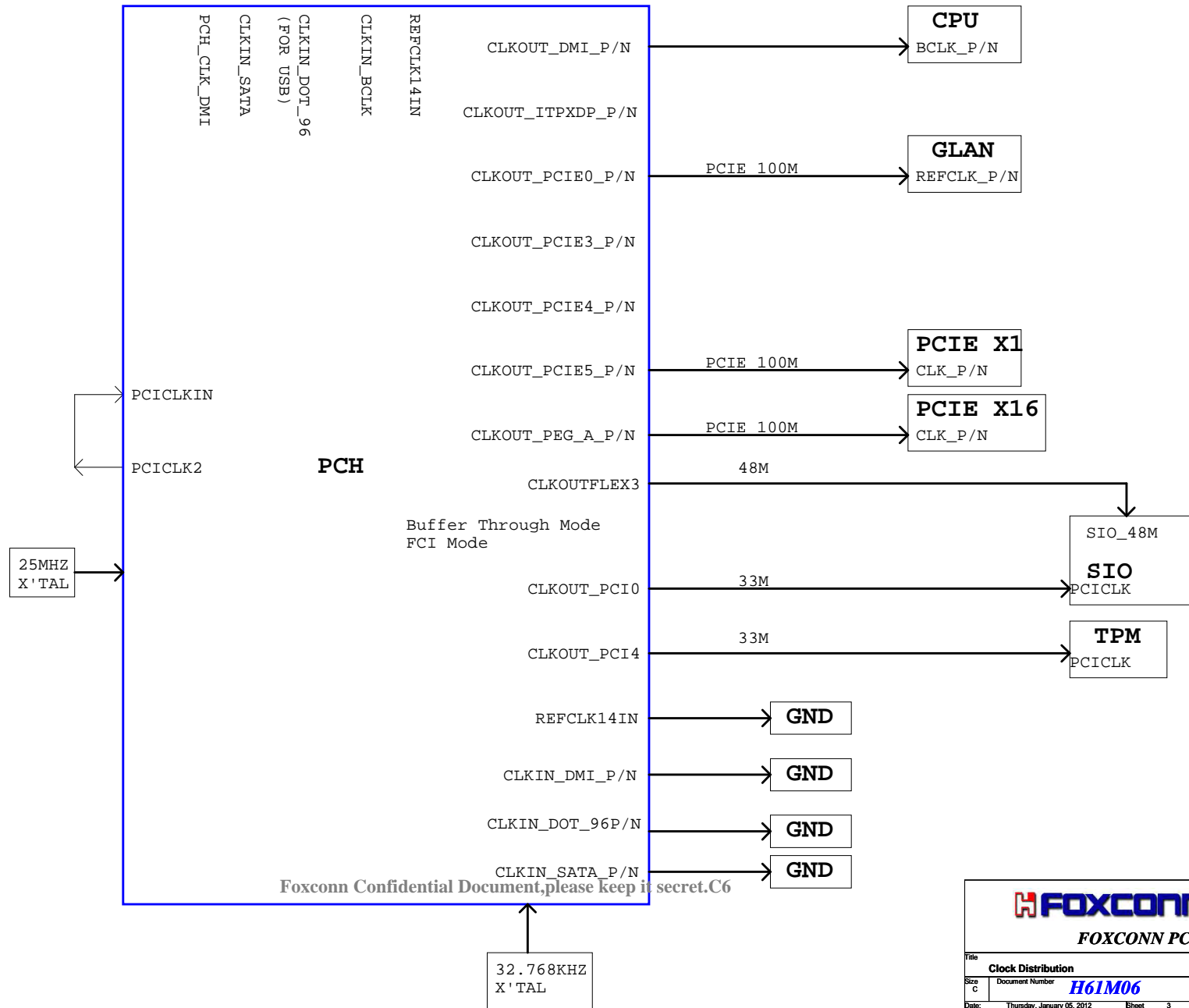
		
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Title <b>Cover Sheet</b>		
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BLOCK DIAGRAM

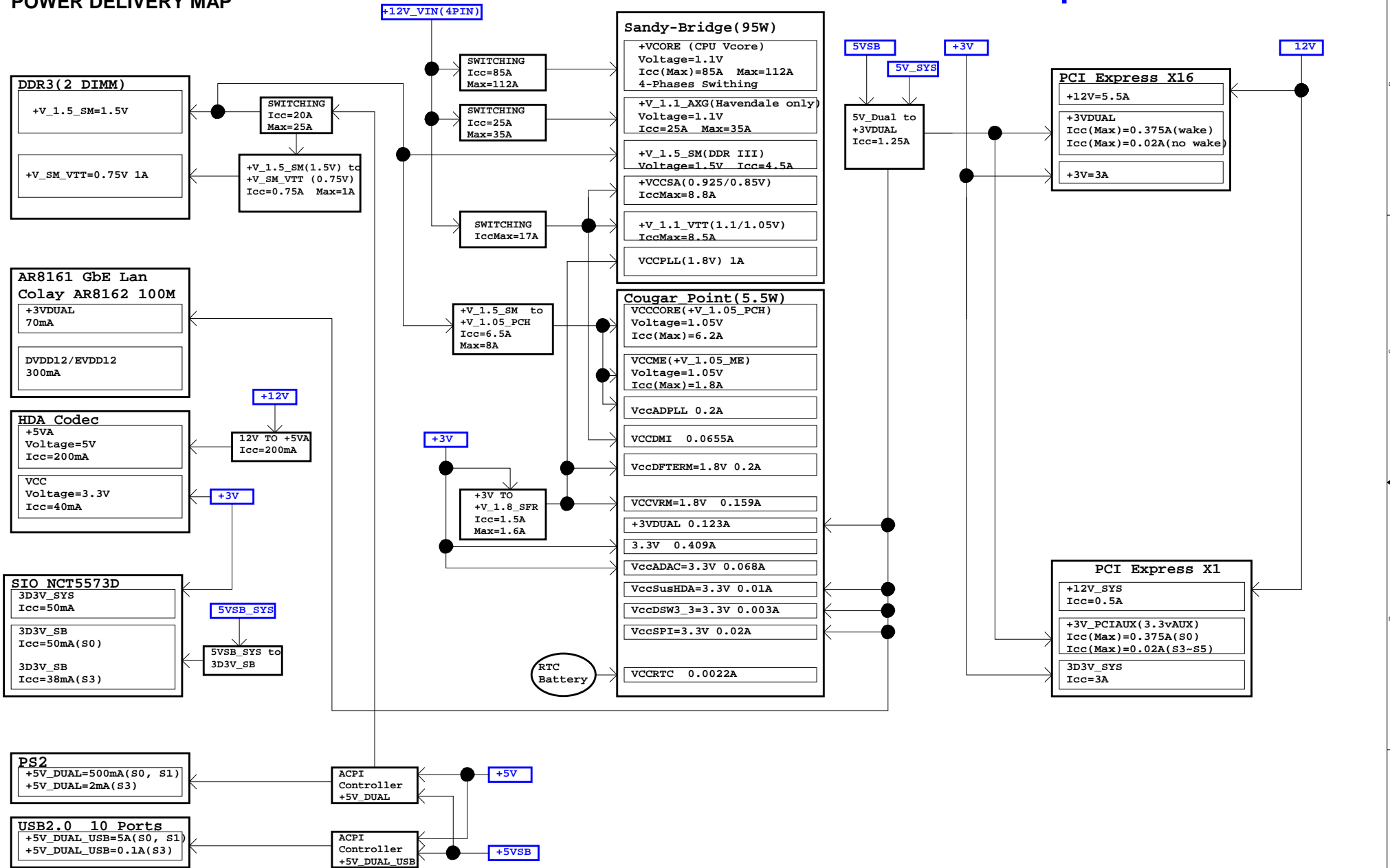


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Title <b>Block Diagram</b>		
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POWER DELIVERY MAP



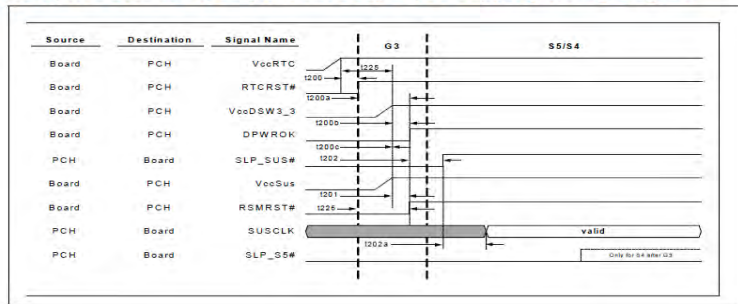
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Title: Power Delivery Map  
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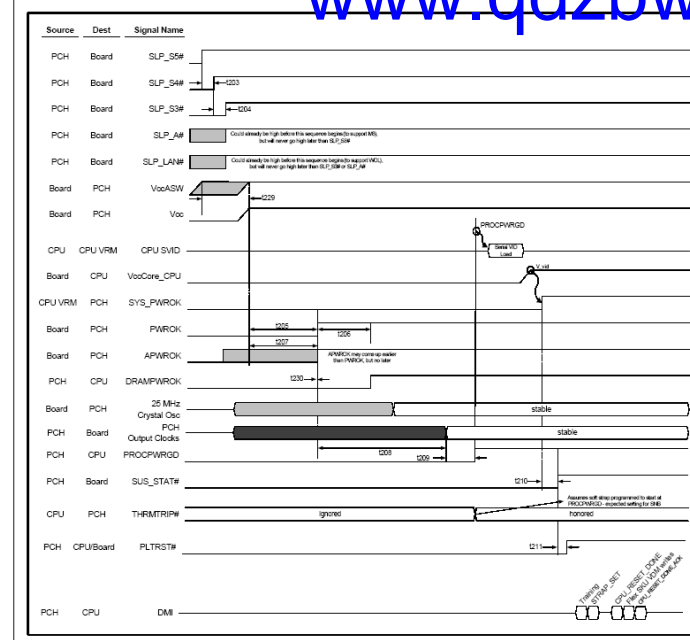
**POWER ON SEQUENCE**

**G3 w/RTC Loss to S4/S5 (Without Deep S4/S5 Support) Timing Diagram**

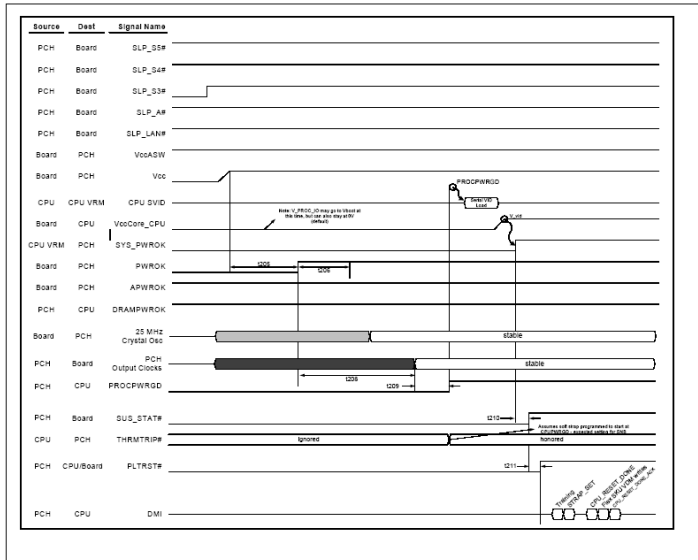


**Figure 8-3. S5 to S0 Timing Diagram**

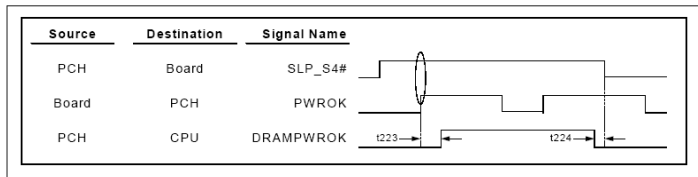
www.qdzbwx.com



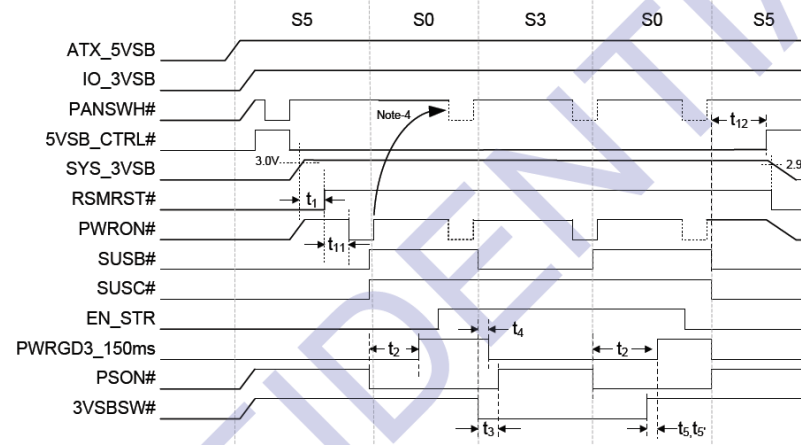
**Figure 8-4. S3/M3 to S0 Timing Diagram**



**Figure 8-8. DRAMPWROK Timing Diagram**



**Figure 11-16. EuP Function Signal Timings**



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File: Power On Sequence  
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RESET / Power Good MAP

Sequence Signal Name:

- (1) O\_PWRBTN#IN
- (2) S\_SLP\_S4# S\_SLP\_S3# S\_SLP\_M#
- (3) O\_PSON#
- (4) B\_ATX\_PWROK
- (5) PCH\_MEPWRGD
- (6) S\_PCH\_SYSPWROK P\_VR\_READY
- (7) PWRGD\_3V
- (8) H\_DRAMPWRGD D3\_RESET#
- (9) H\_PWRGD
- (10) S\_PLTRST# H\_RESET#\_R S\_PLTRST#\_R
- (11) X\_PLTRST\_PCIE\_SLOT# K\_PCIRST#\_SLOT
- (12) A\_Z\_RST#

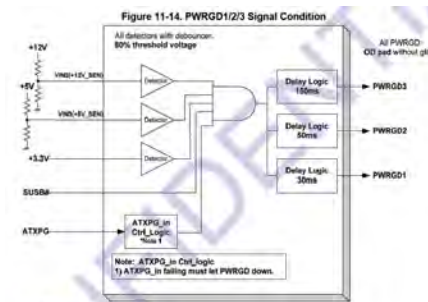
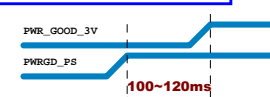
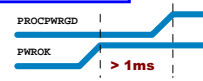
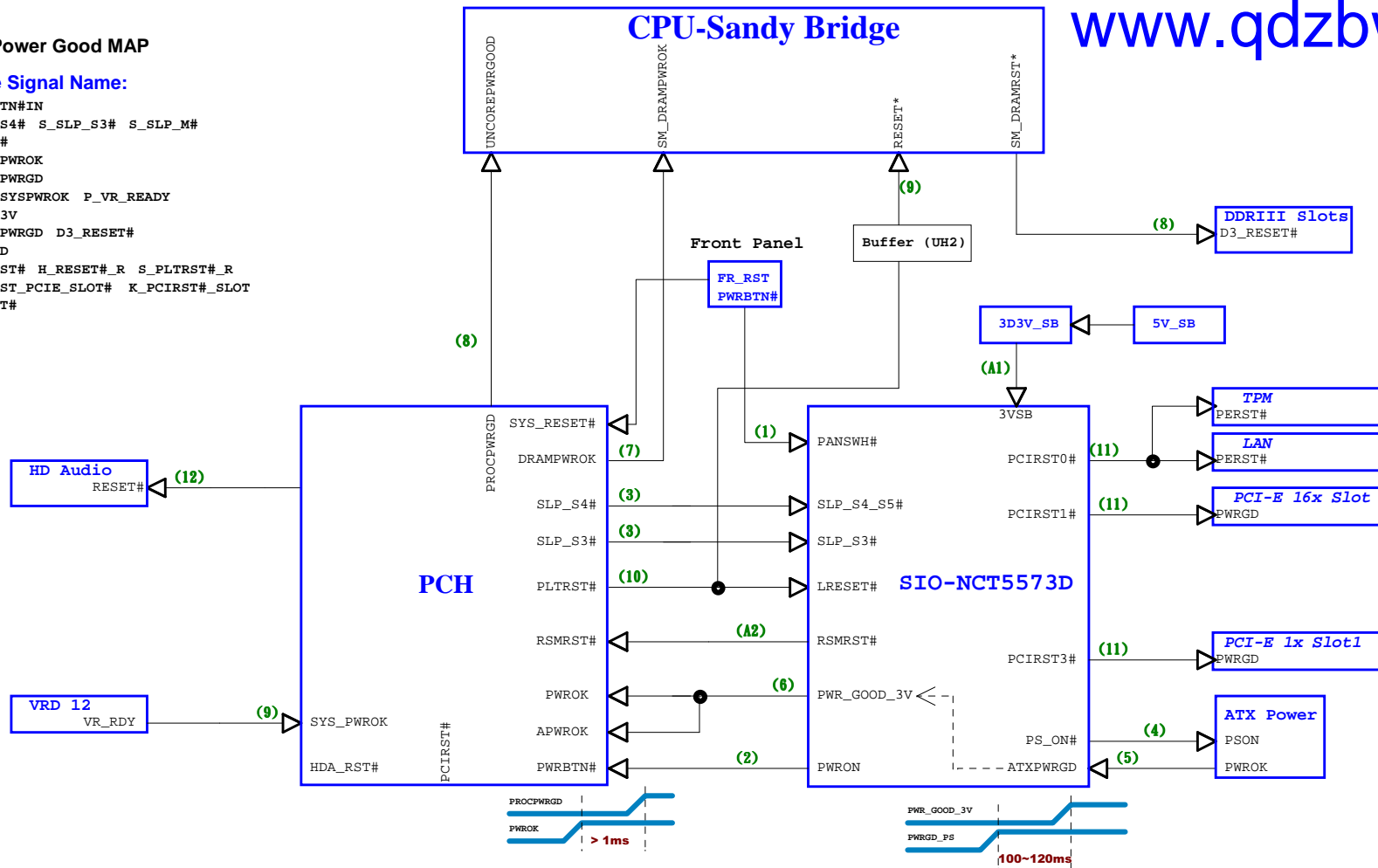


Figure 11-15. PWRGD1/2/3 Signal Timings

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Title: Reset/power good  
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IRQ Routing Table

	INTA#	INTB#	INTC#	INTD#	IDSEL	REQn#	GNTn#
Slot1	A	B	C	D	16	0	0


	INTA#	INTB#	INTC#	INTD#	IDSEL	REQn#	GNTn#
Slot2	B	C	D	A	17	2	2

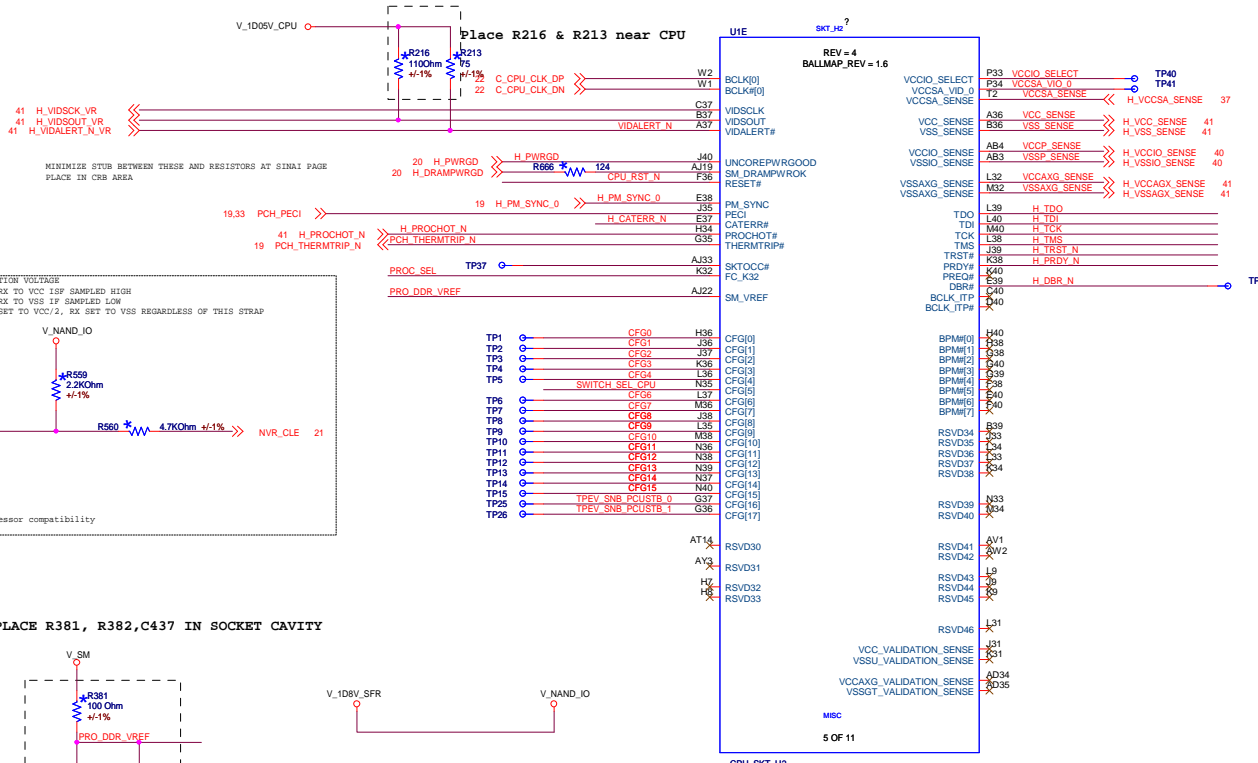
STRAPPING Table

CPU side

CFG[17:0]	Description	
[2]	PCI Express static x16 lane numbering reversal	1: normal <b>Default</b> 0: lane numbers reversed
[6:5]	PCI Express Bifurcation	00: 1x8, 2x4 PCI Express 01: reserved 10: 2x8 PCI Express 11: 1x16 PCI Express <b>Default</b>

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 <b>FOXCONN PCEG</b>		
Title <b>STRAP</b>		
Size C	Document Number <b>H61M06</b>	Rev A
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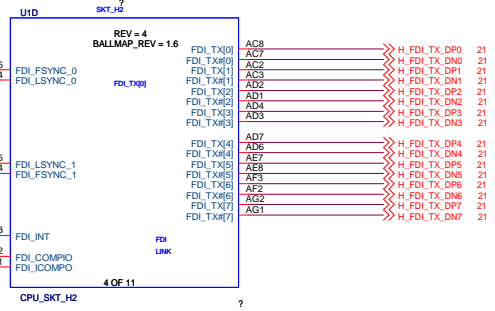
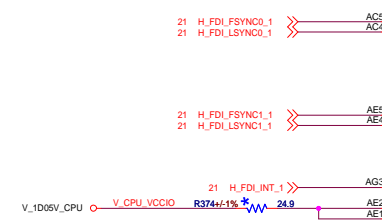
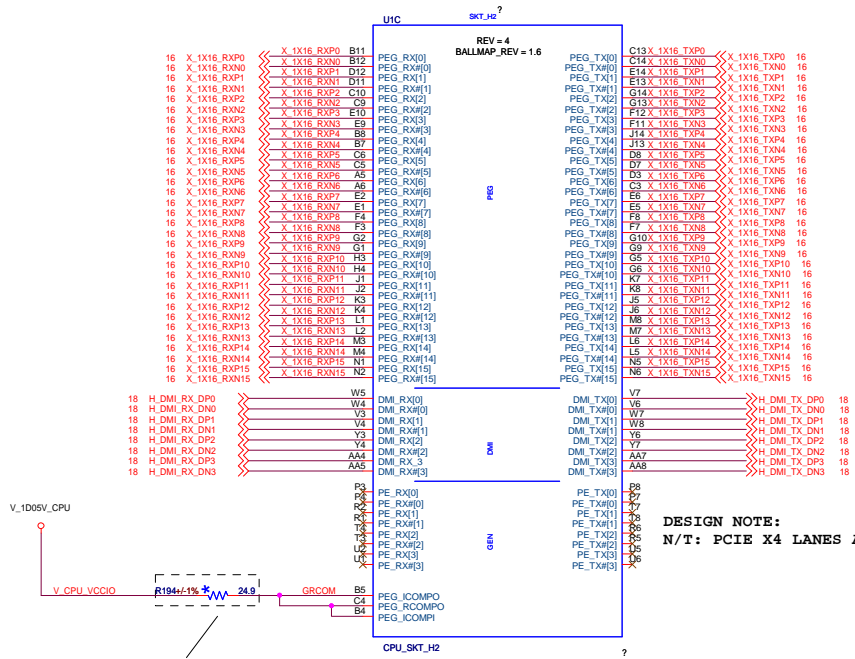
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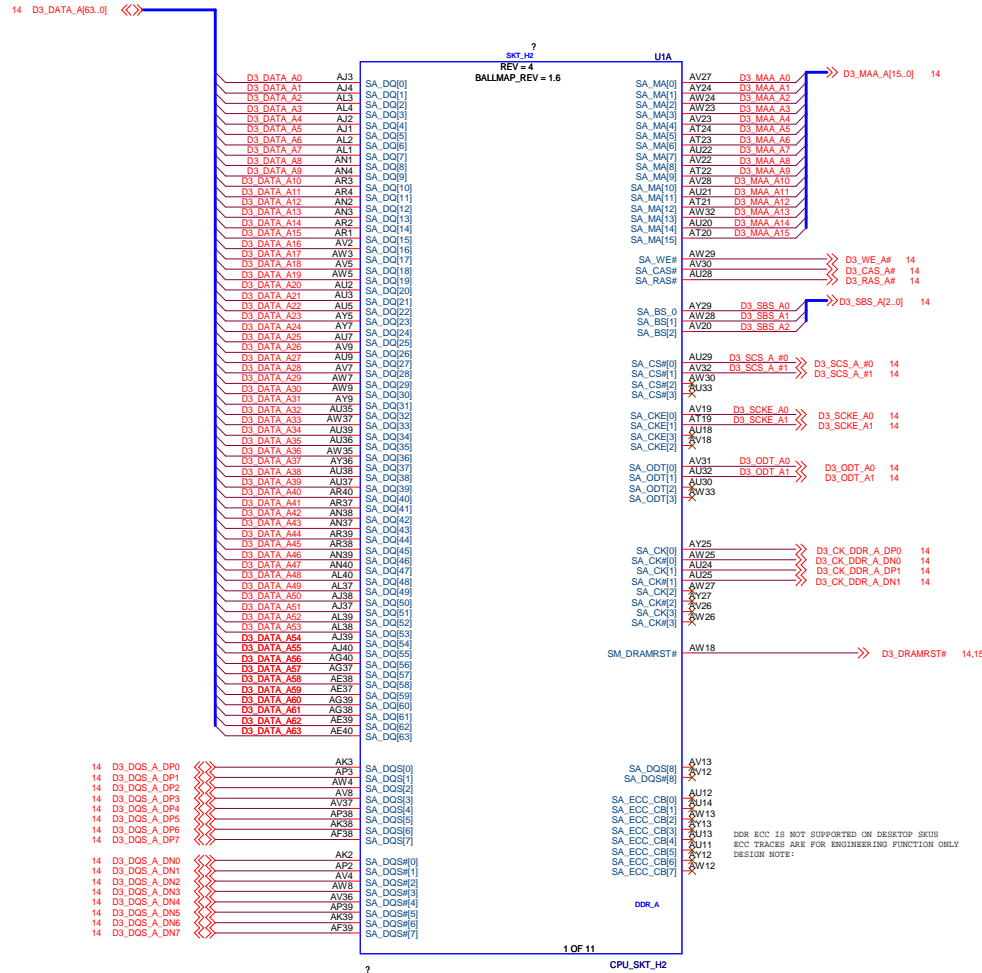


DESIGN NOTE:  
N/T: PCIE X4 LANES ARE NOT SUPPORTED ON DESKTOP CPU SKUS

Short B4 & C4 together, route as a single 4 mil trace to R2  
Route B5 to R2 as a separate 10 mil trace

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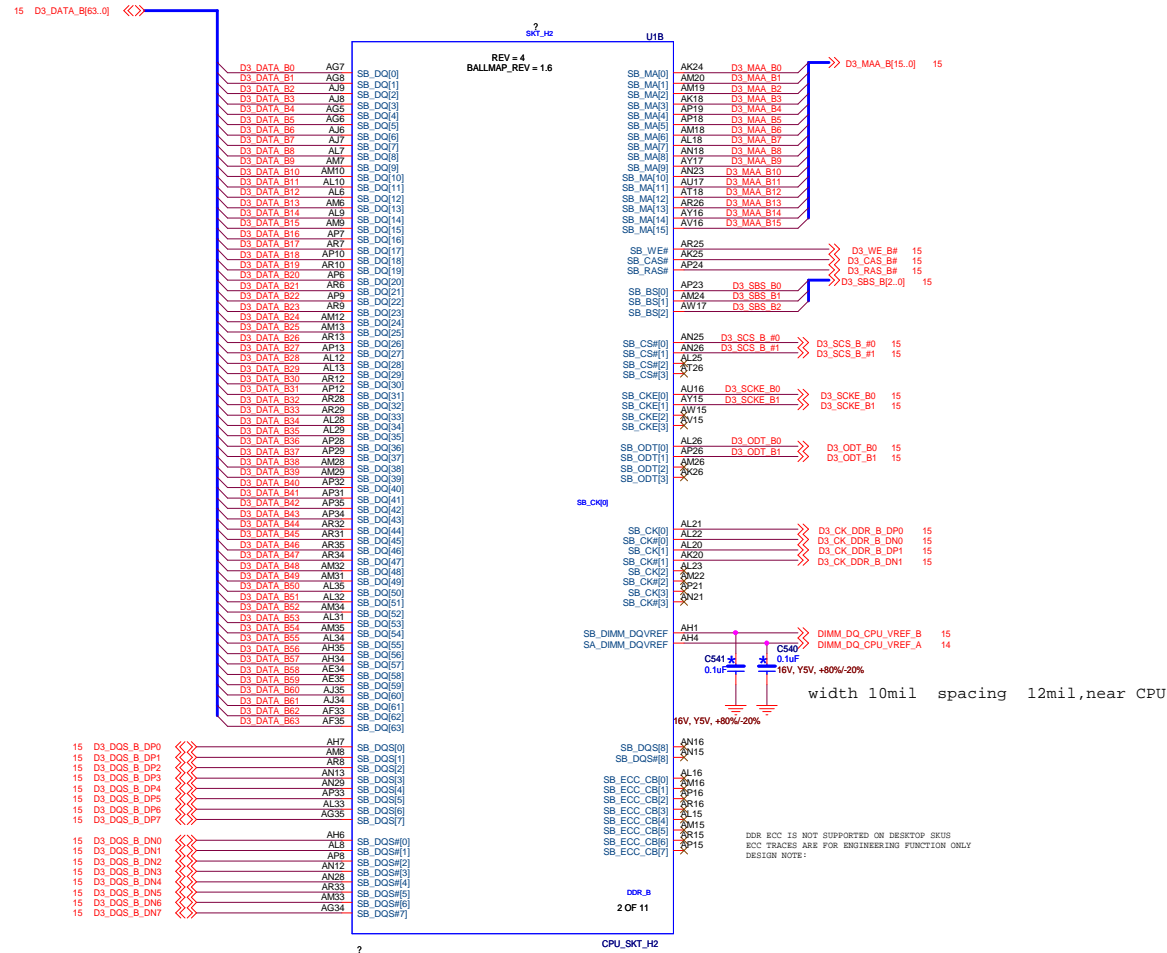
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Title: **CPU3-DDR3\_CHA**

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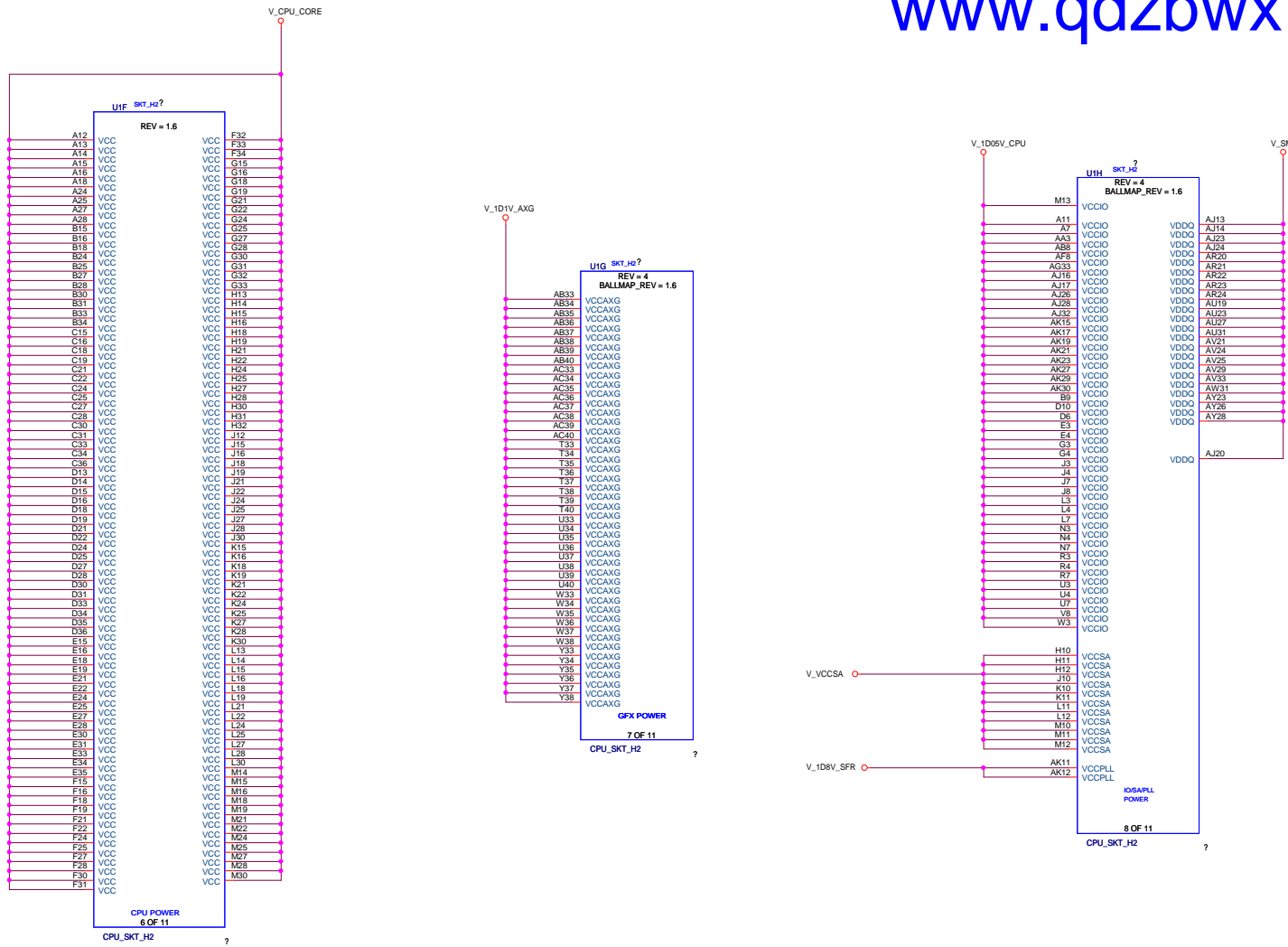
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Title  
**CPU4-DDR3\_CHB**

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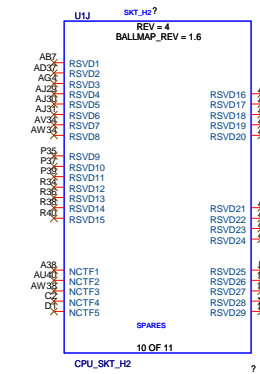
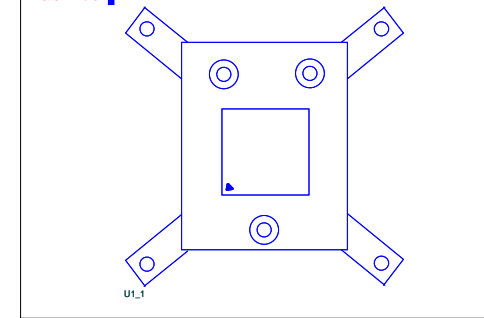
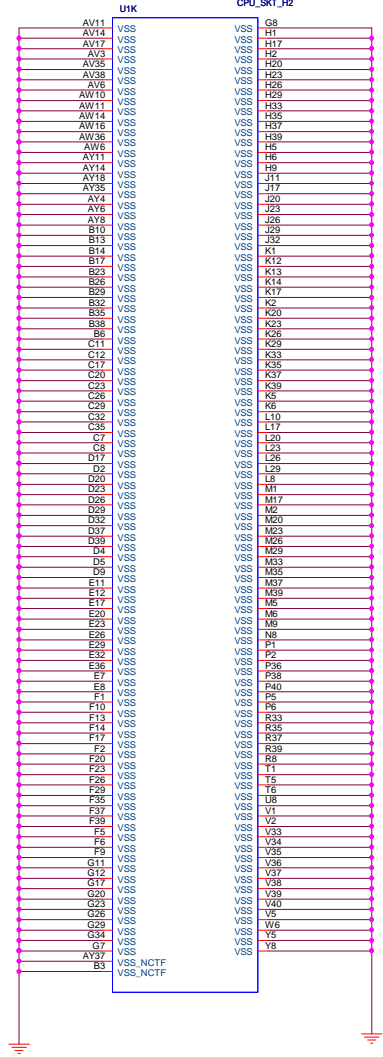
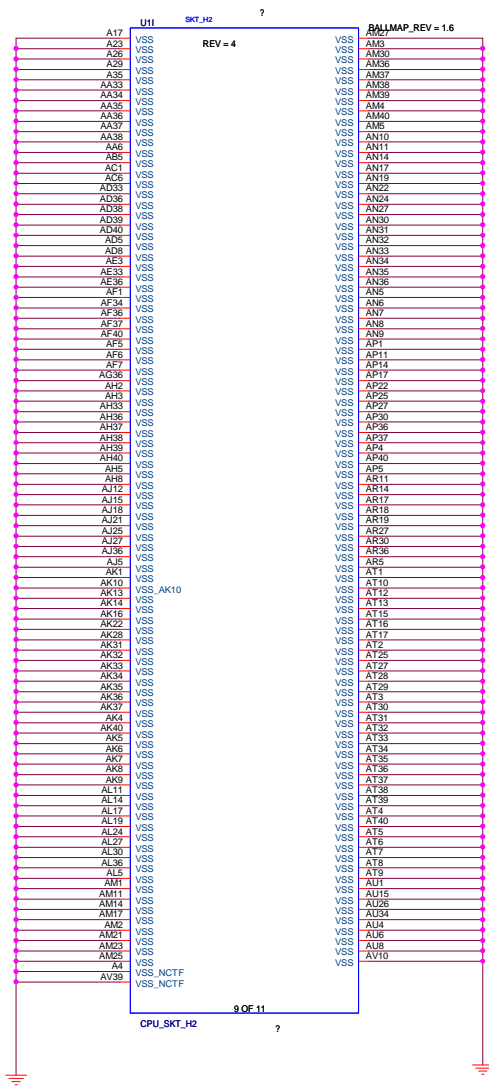
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Title  
**CPUS-POWER**

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Fab 1.0

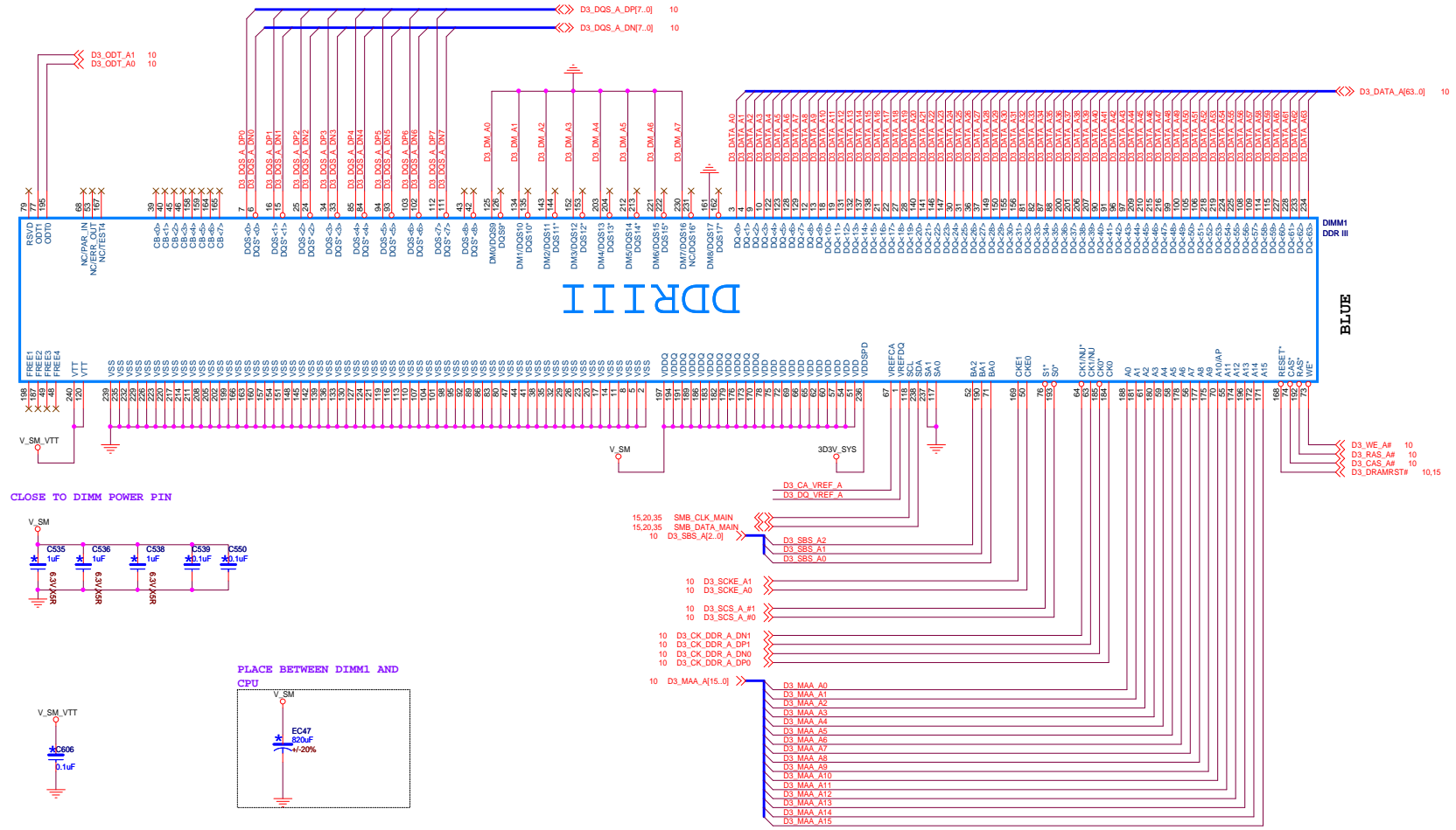


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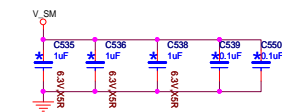
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Title: CPU6-GND  
 Size: C Document Number: **H61M06** Rev: A  
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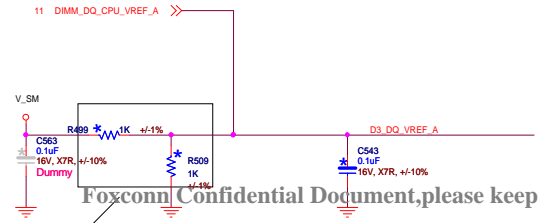
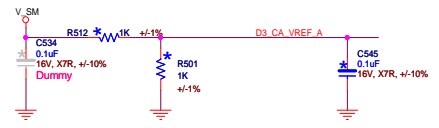
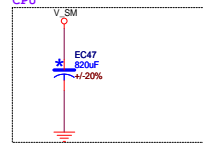
CHANNEL A DIMM 1  
SMB ADDRESS:000



CLOSE TO DIMM POWER PIN



PLACE BETWEEN DIMM1 AND CPU



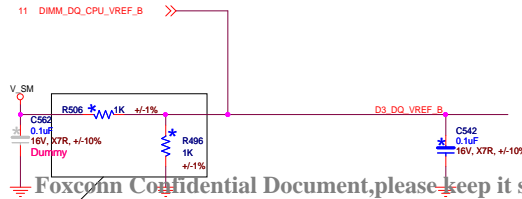
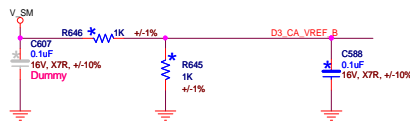
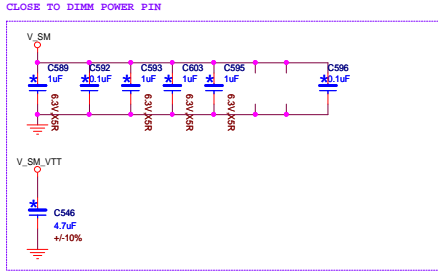
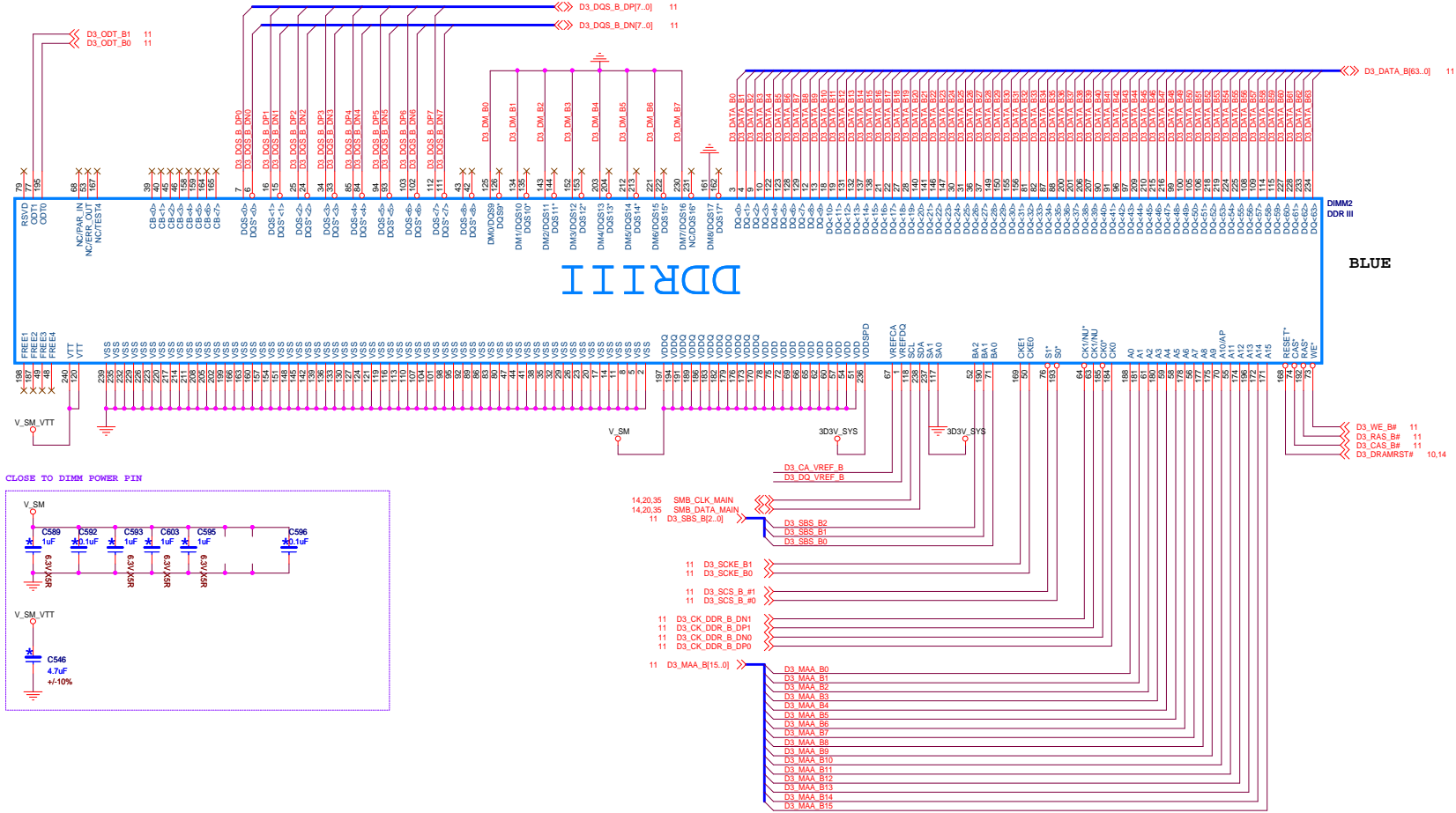
PLACE RESISTORS CLOSE TO CHL\_A DIMMS ON DIMM\_VREF\_A

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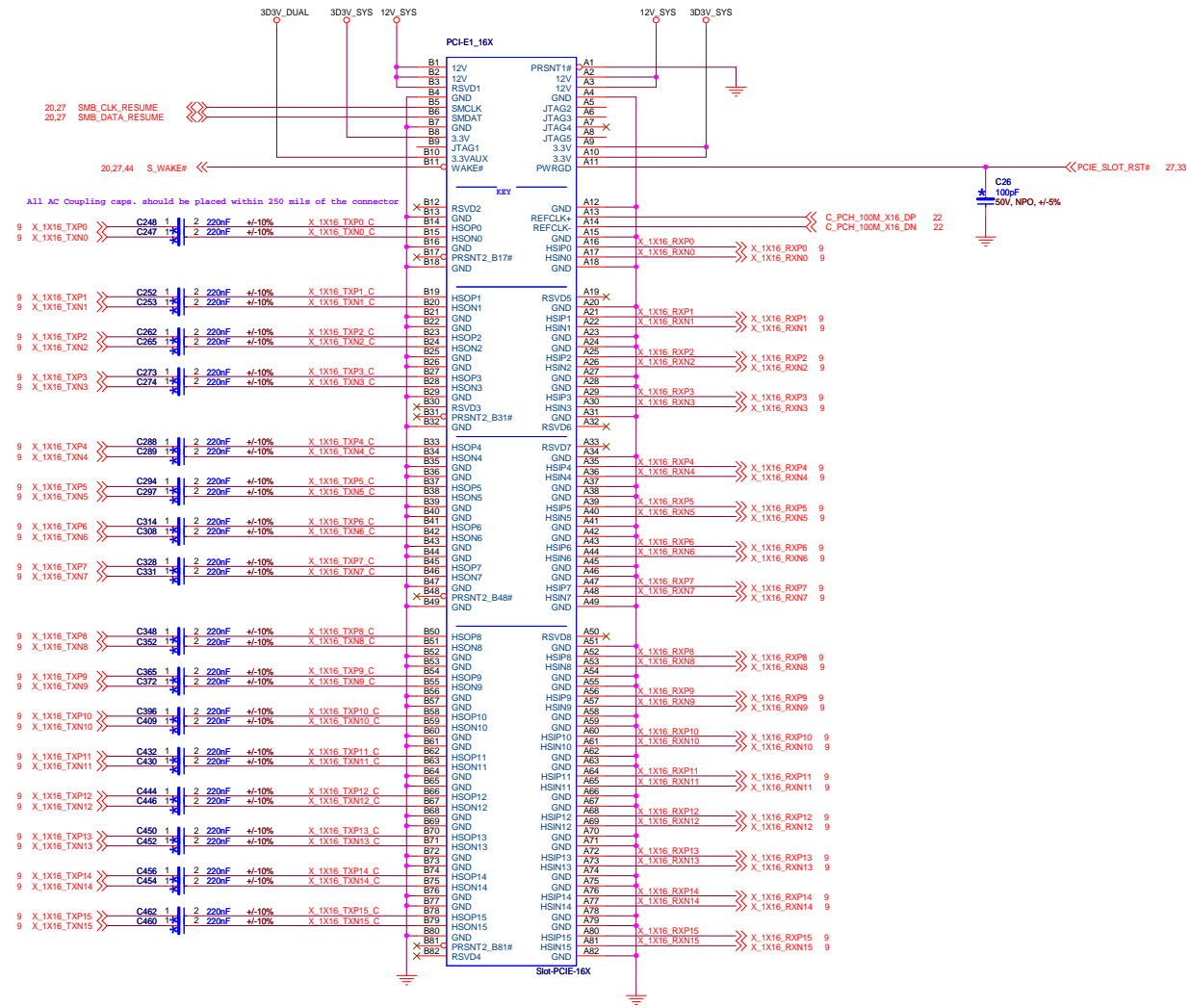
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Size: C Document Number: H61M06 Rev: A  
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CHANNEL B DIMM 3  
SMB ADDRESS:010



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PLACE RESISTORS CLOSE TO CH\_B DIMMS  
ON DIMM\_VREF\_B



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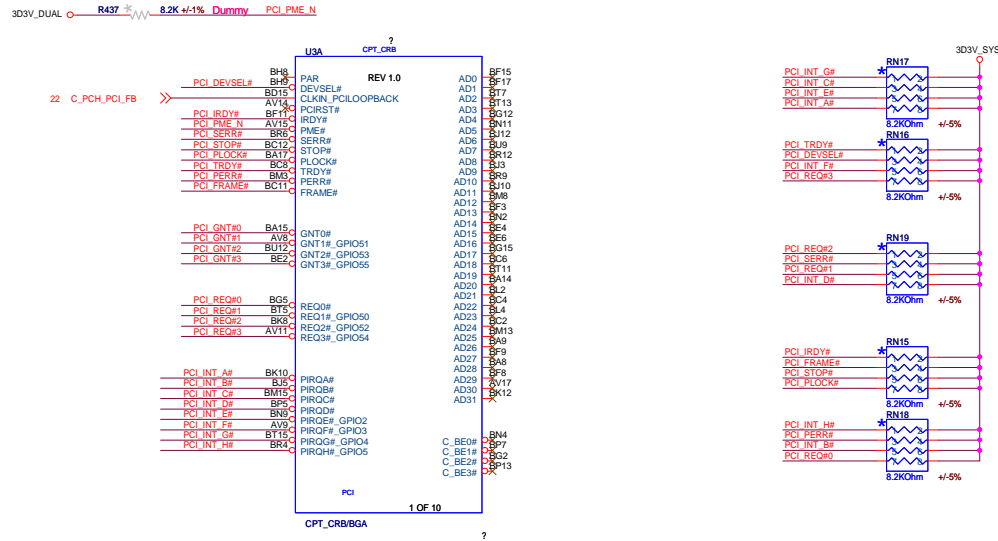
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Title: **PCIE X16/X1**

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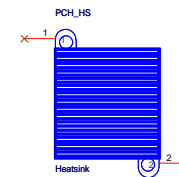
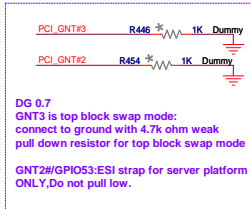


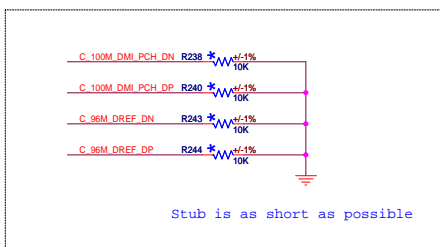
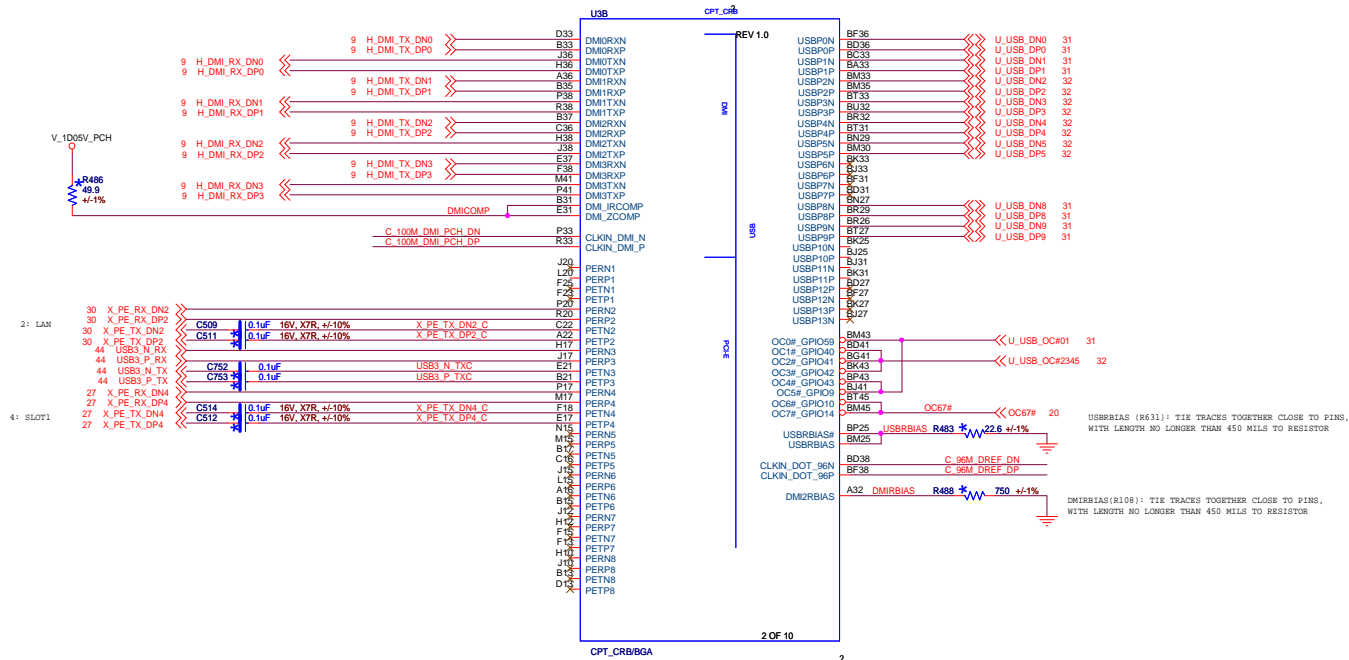


STRAP: Boot BIOSselect check whether GNT1 or SATA1GP (GPIO19)

BOOT DEVICE	GNT1	SATA1GP
LPC	0	0
NAND	0	1
PCI	1	0
SPI	1	1

PCI\_GNT#0 R445 1K Dummy  
 PCI\_GNT#1 R438 1K Dummy  
 Internal pull-up





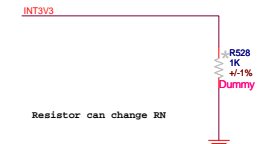
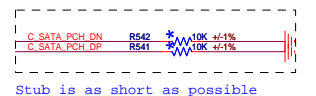
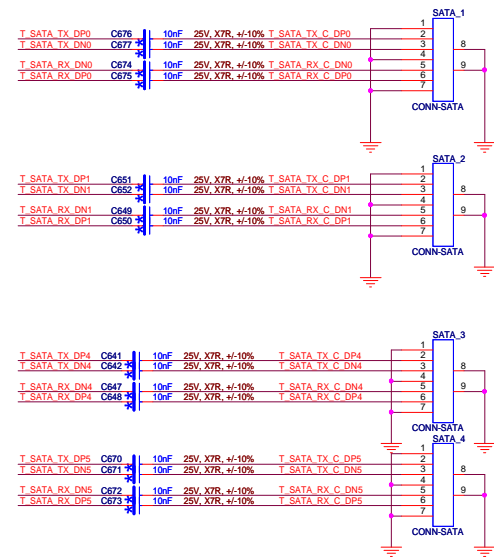
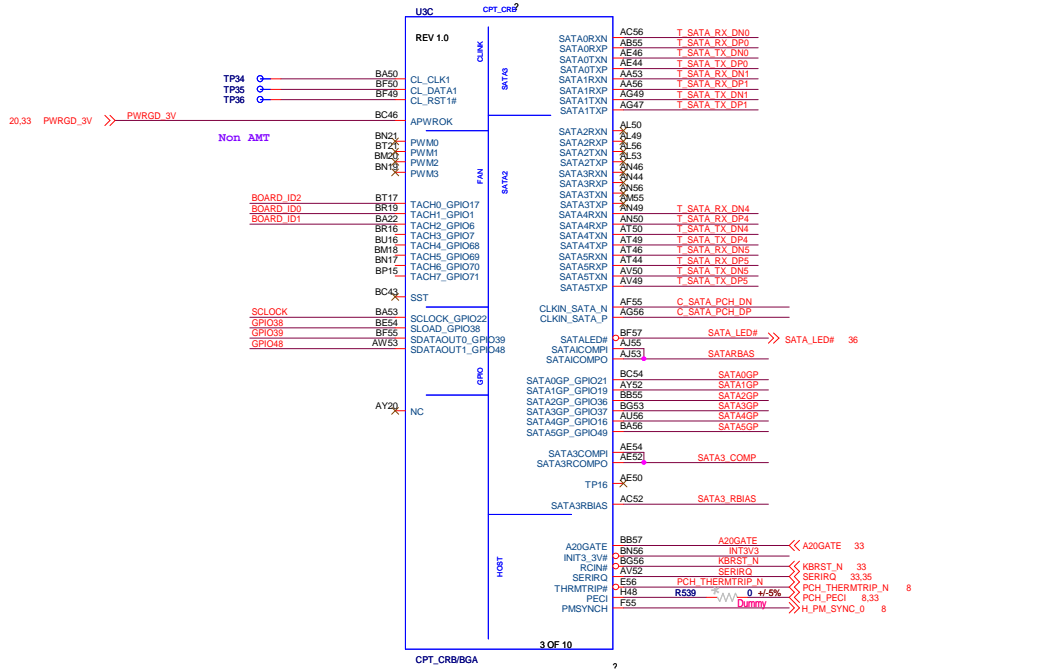
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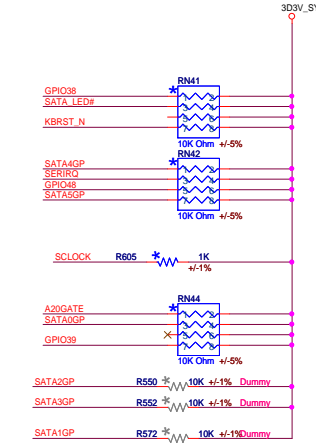
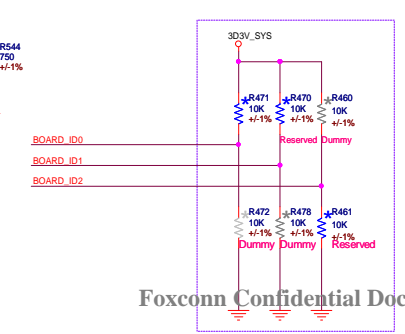
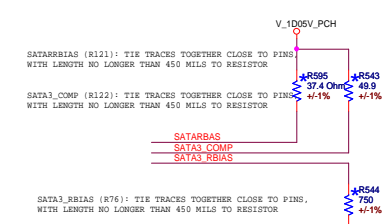
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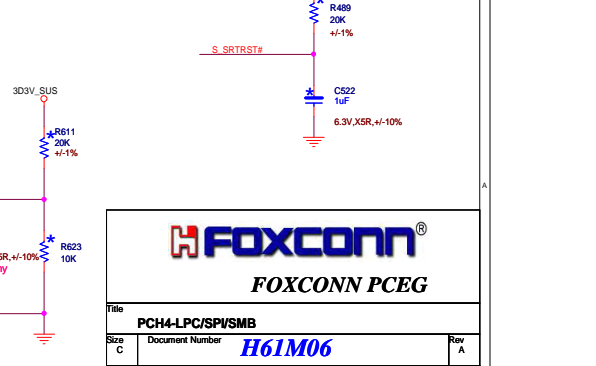
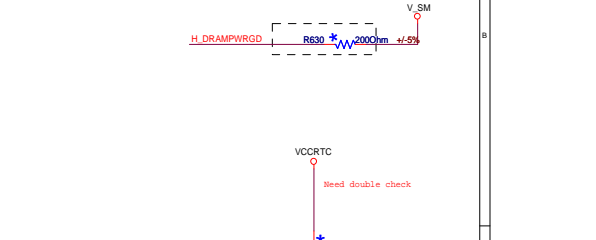
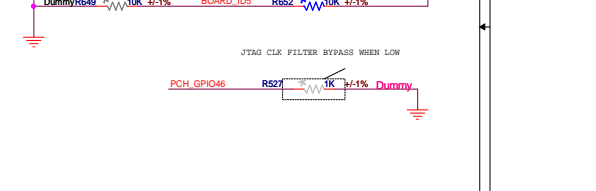
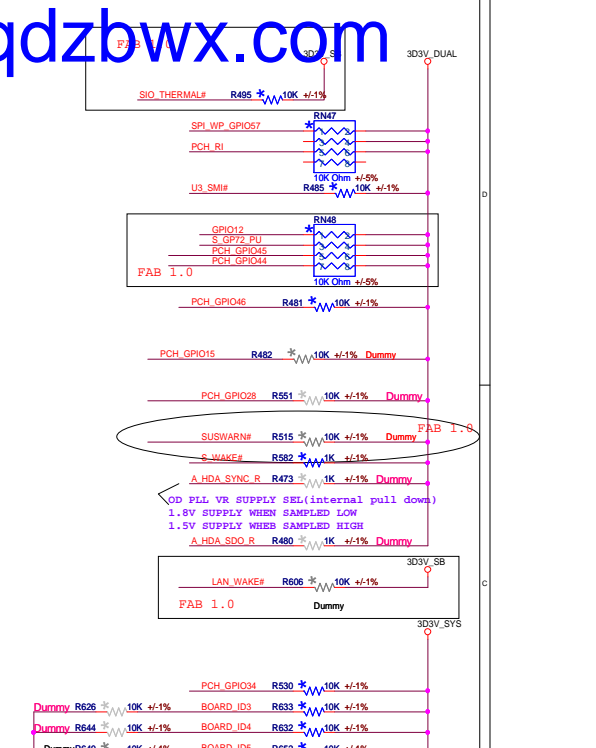
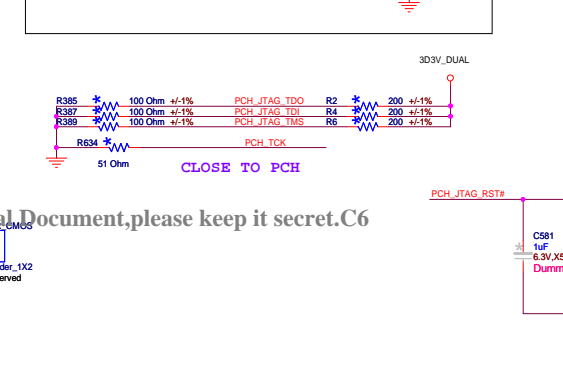
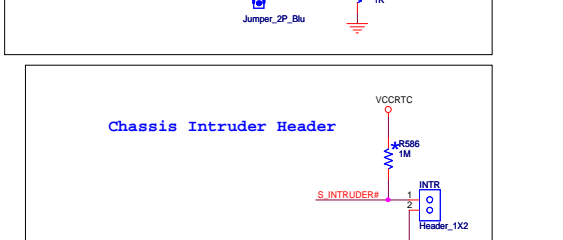
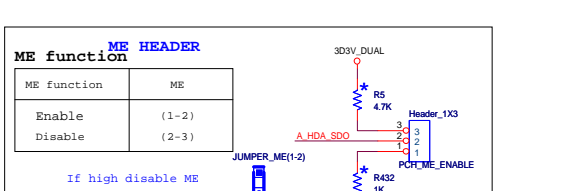
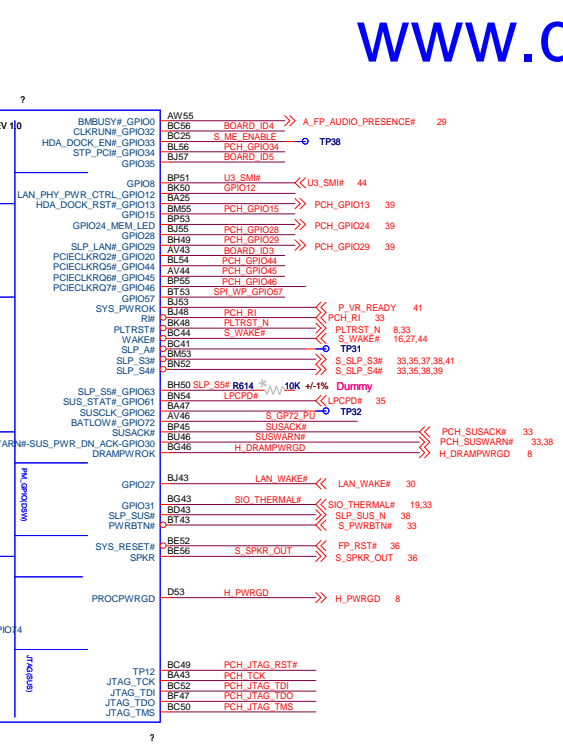
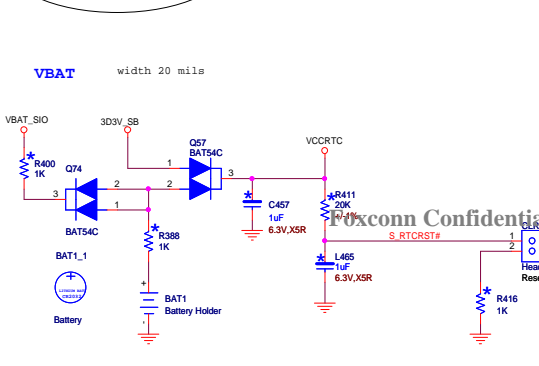
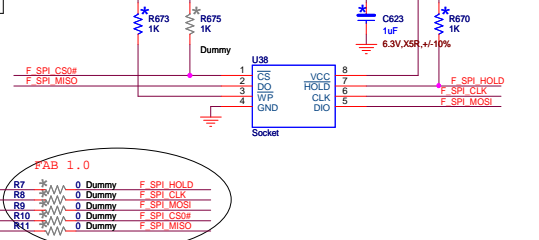
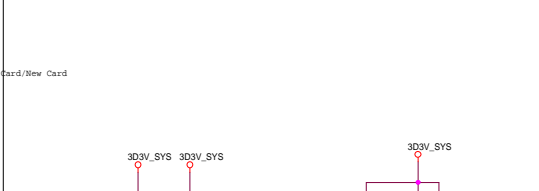
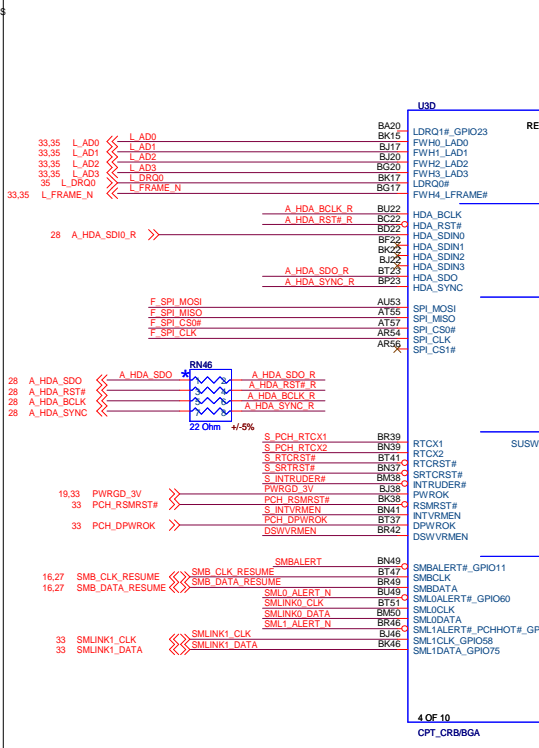
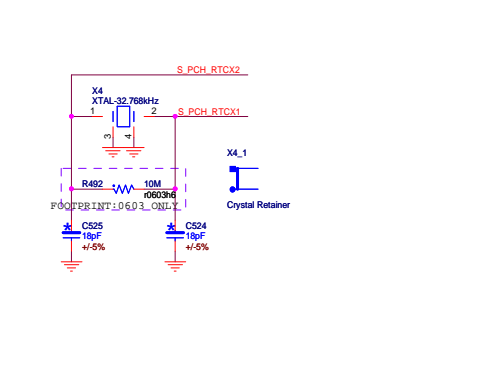
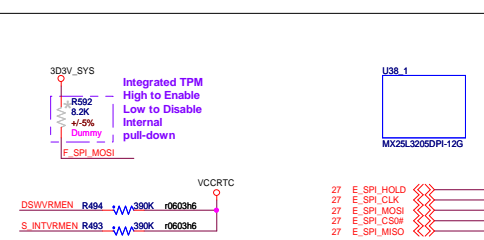
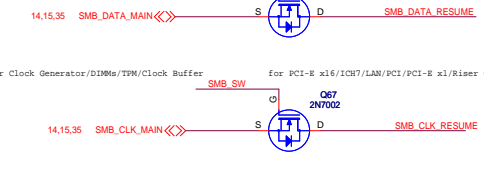
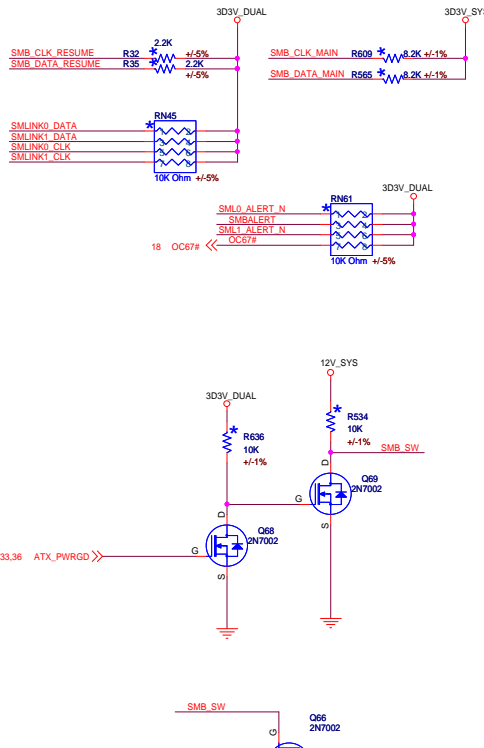
Need double check



BOARD\_ID2 BOARD\_ID1 BOARD\_ID0

H61MXE-S	0	0	1
H61MXE	0	1	0
H61MXE-V	0	1	1

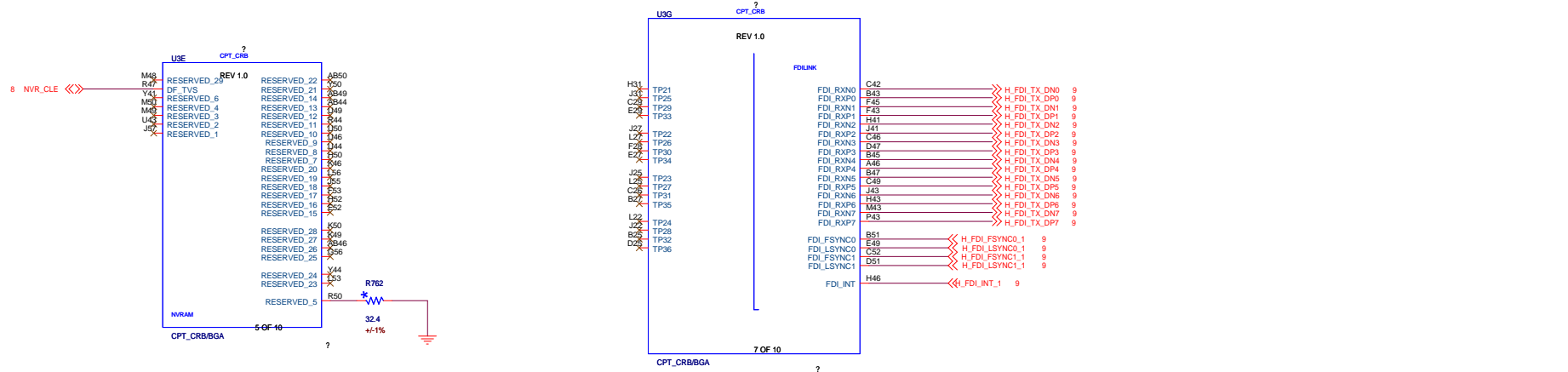
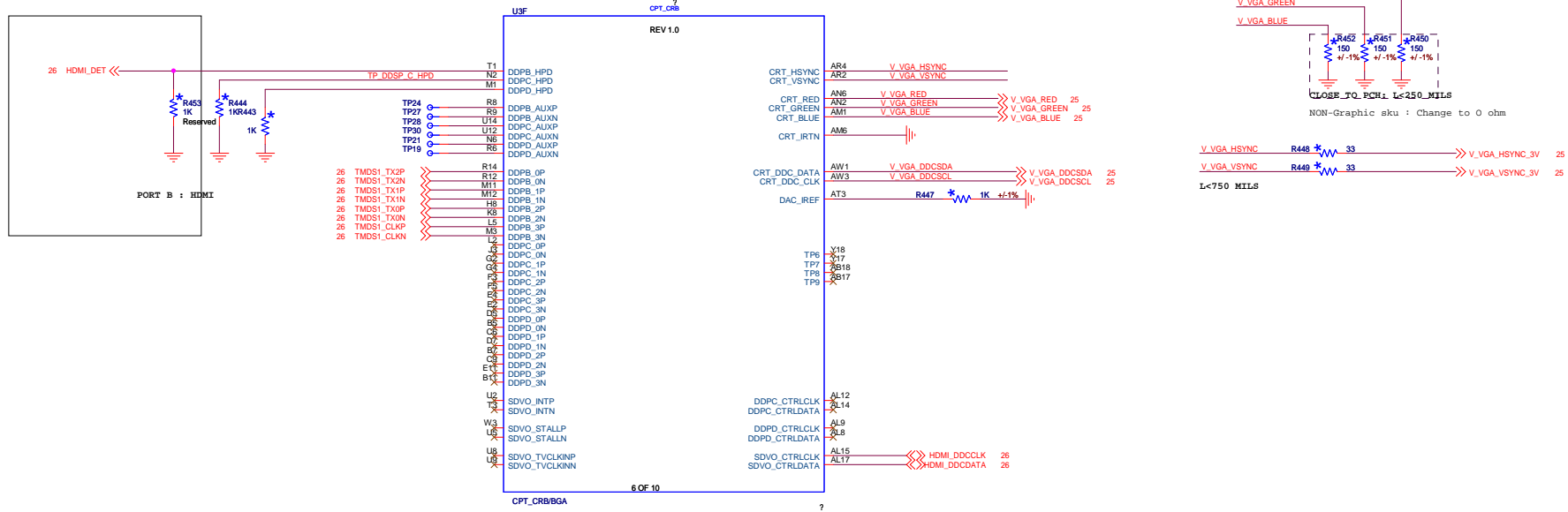
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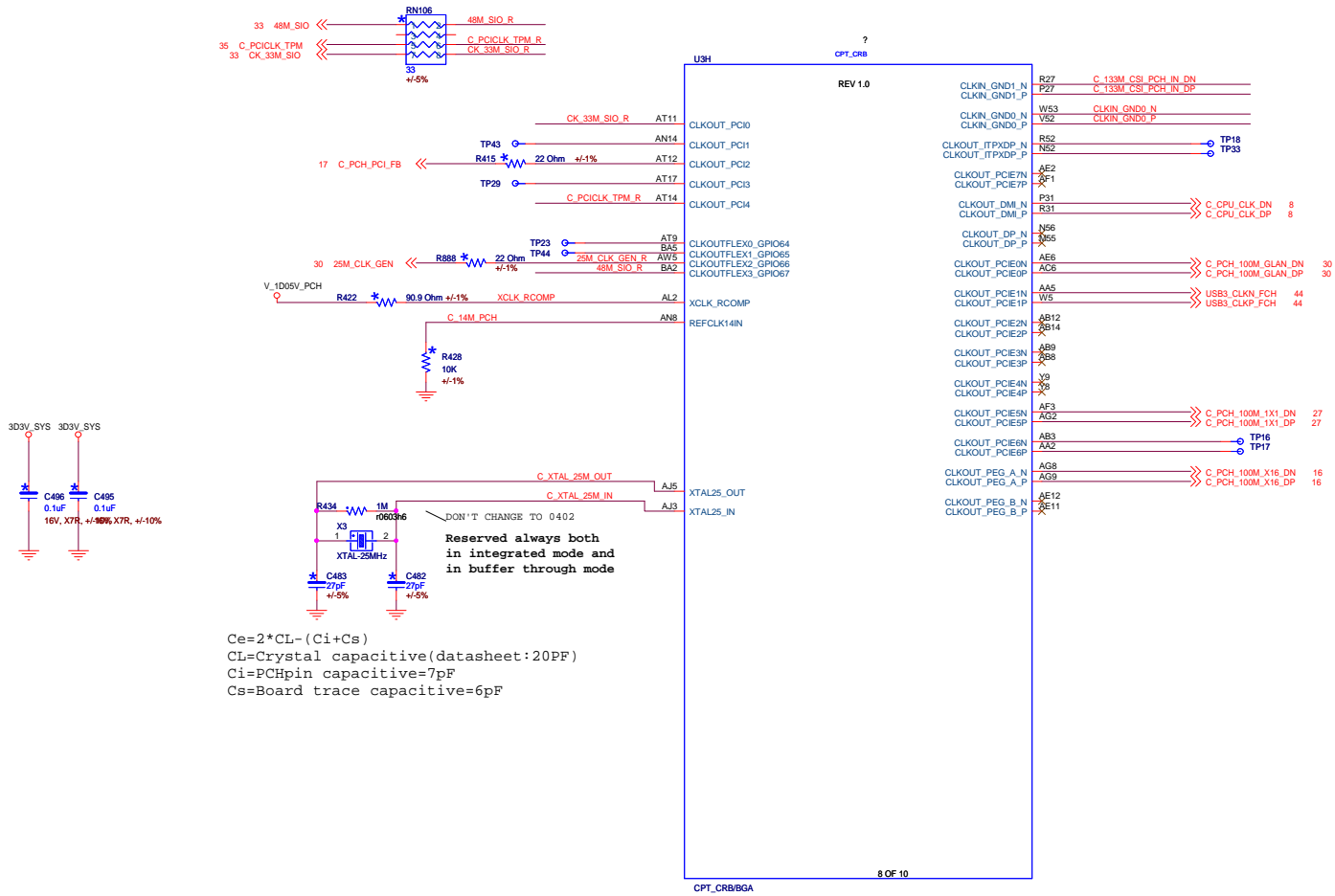
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FOXCONN PCEG

Title: PCH5-NVAND/FDI/DISPLAY  
 Size C Document Number H61M06 Rev A  
 Date: Thursday, January 05, 2012 Sheet 21 of 45



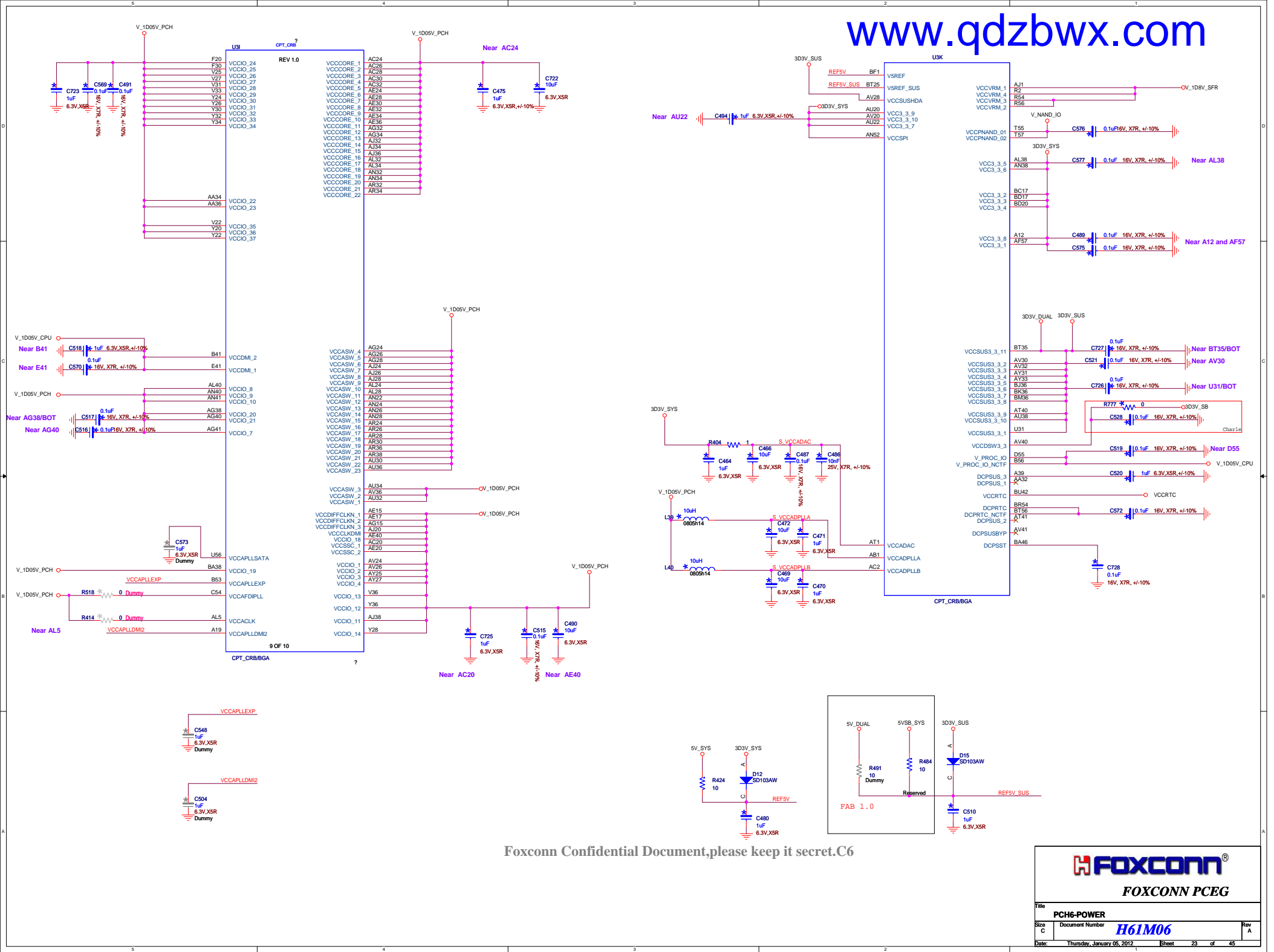
Stub is as short as possible



$C_e = 2 * C_L - (C_i + C_s)$   
 $C_L = \text{Crystal capacitance (datasheet: 20PF)}$   
 $C_i = \text{PCHpin capacitance} = 7\text{pF}$   
 $C_s = \text{Board trace capacitance} = 6\text{pF}$

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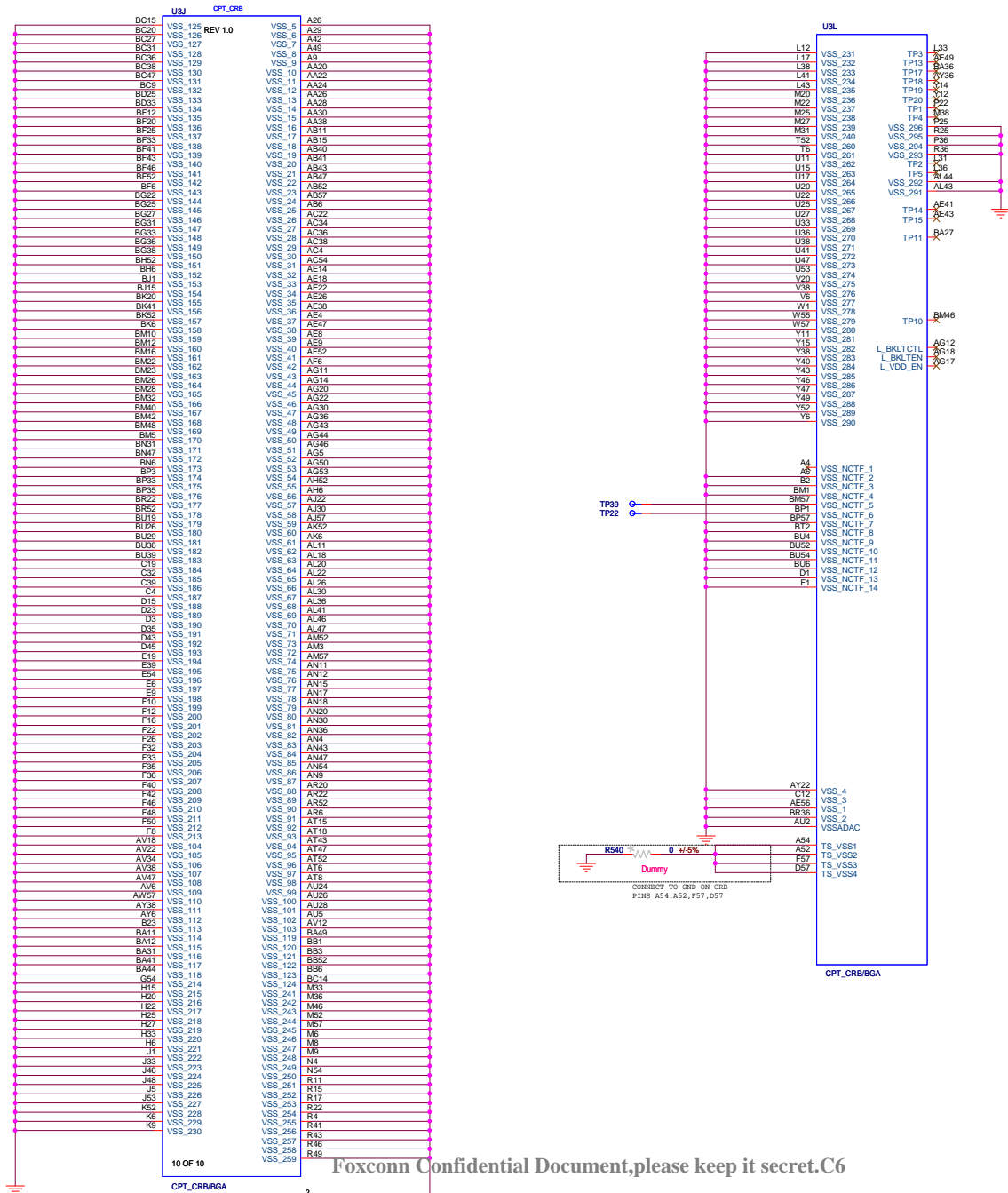
<b>FOXCONN®</b>		
<b>FOXCONN PCEG</b>		
Title <b>PCH8-CLOCK</b>		
Size C	Document Number <b>H61M06</b>	Rev A
Date: Thursday, January 05, 2012	Sheet 22	of 45



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FOXCONN PCEG

Title: PCH6-POWER  
 Size C: Document Number H61M06 Rev A  
 Date: Thursday, January 05, 2012 Sheet 23 of 45



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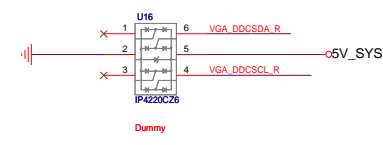
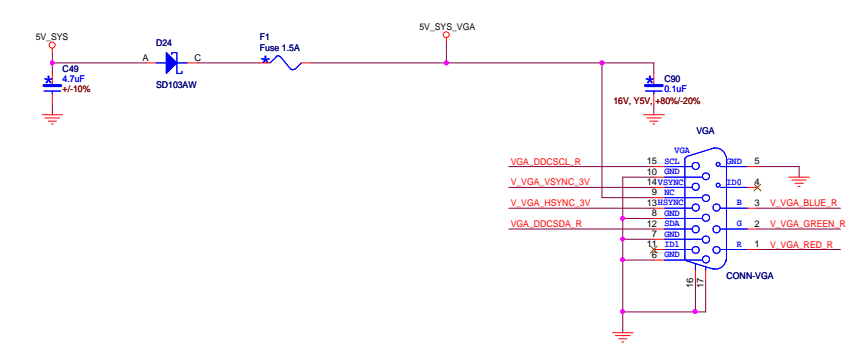
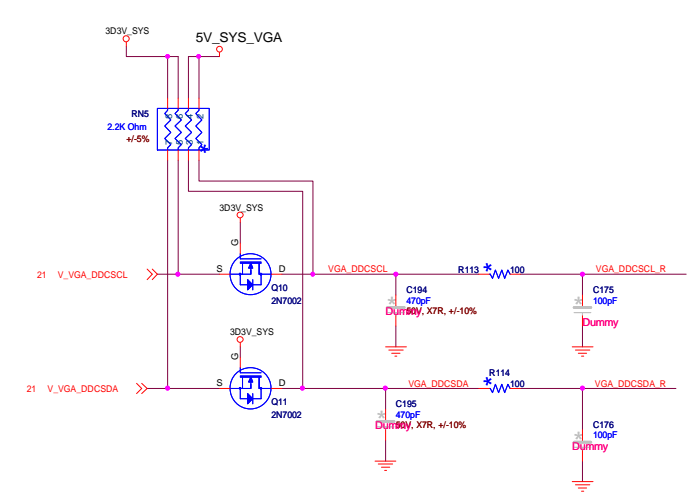
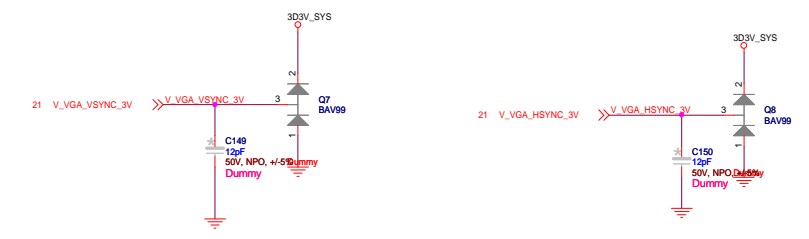
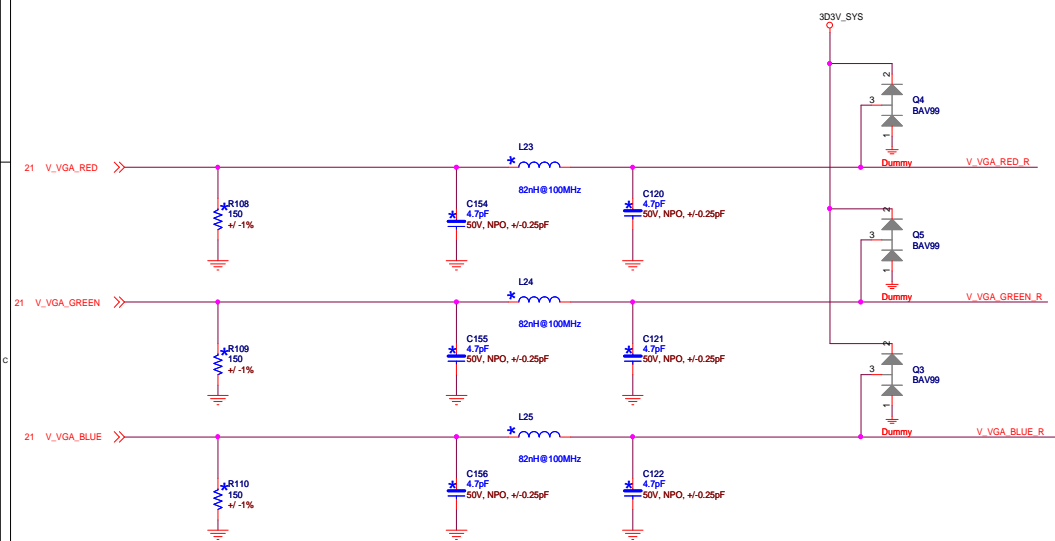
**FOXCONN**  
FOXCONN PCEG

Title: PCH7-GND

Size C Document Number: H61M06 Rev A

Date: Thursday, January 05, 2012 Sheet 24 of 45





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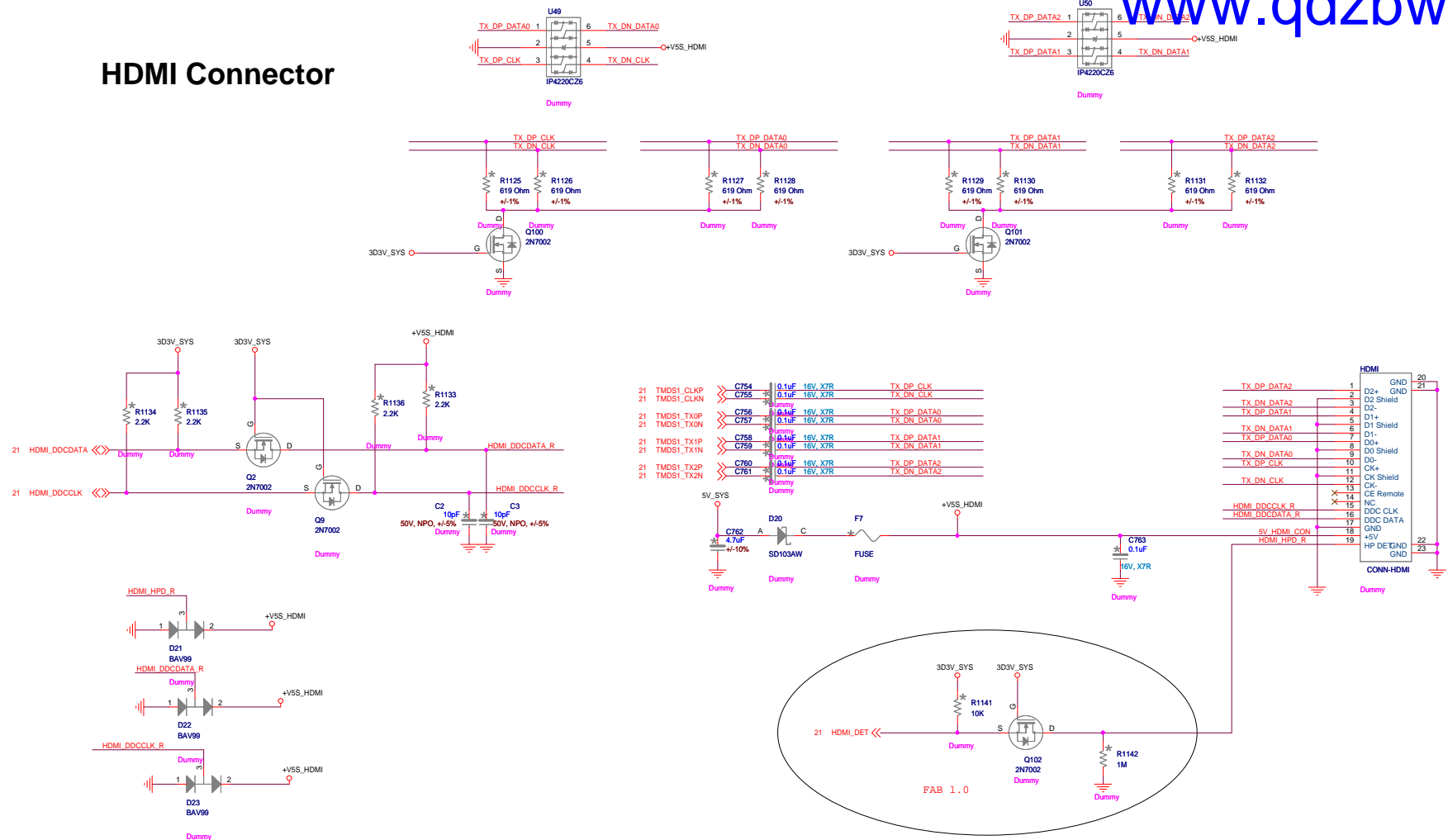
**FOXCONN**  
FOXCONN PCEG

Title: **VGA**

Size: C Document Number: **H61M06** Rev: A

Date: Thursday, January 05, 2012 Sheet: 25 of 45

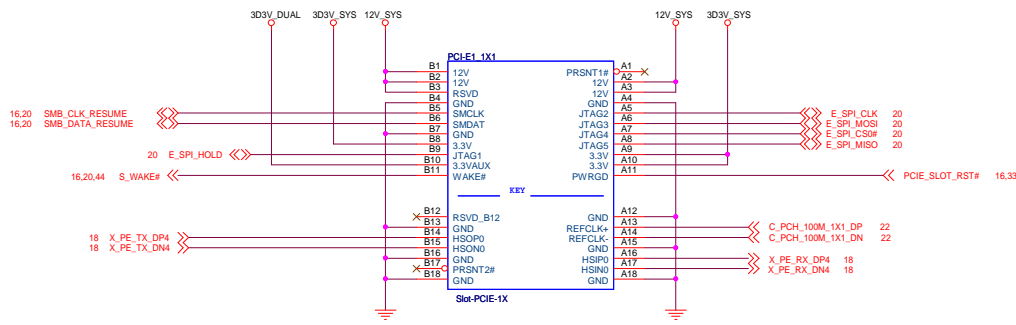
# HDMI Connector



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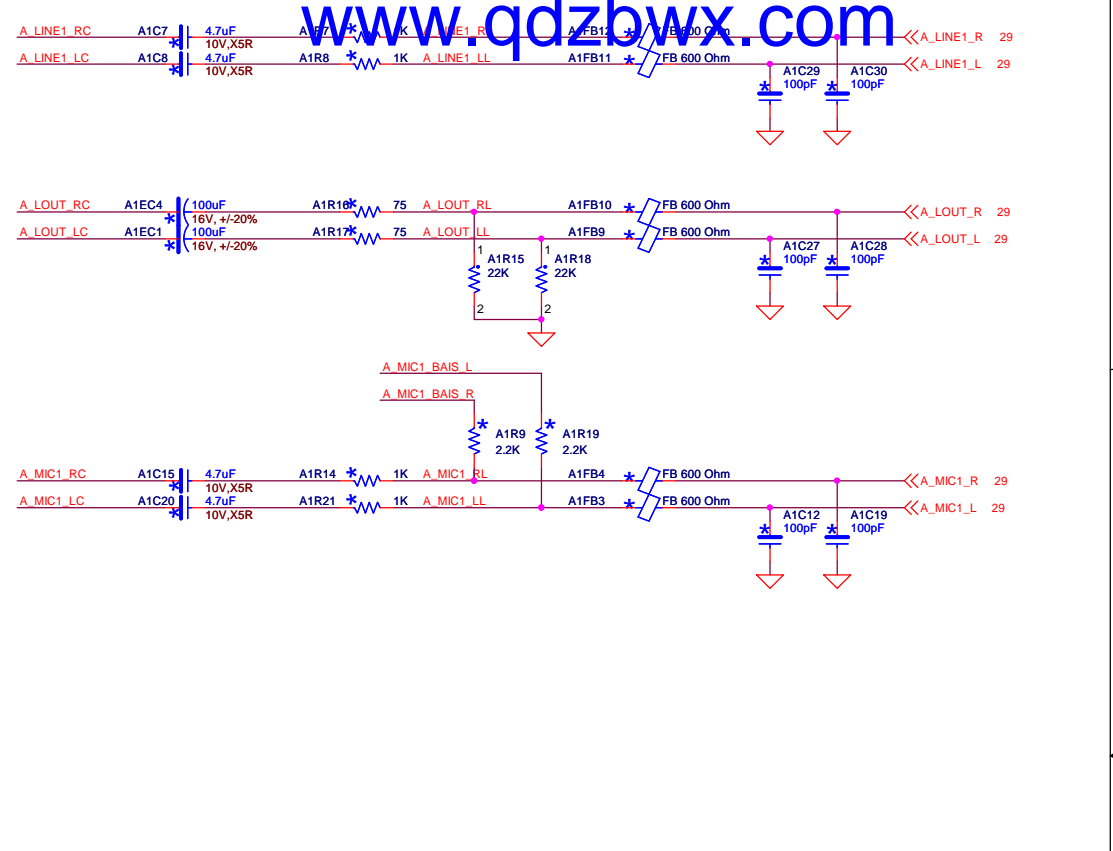
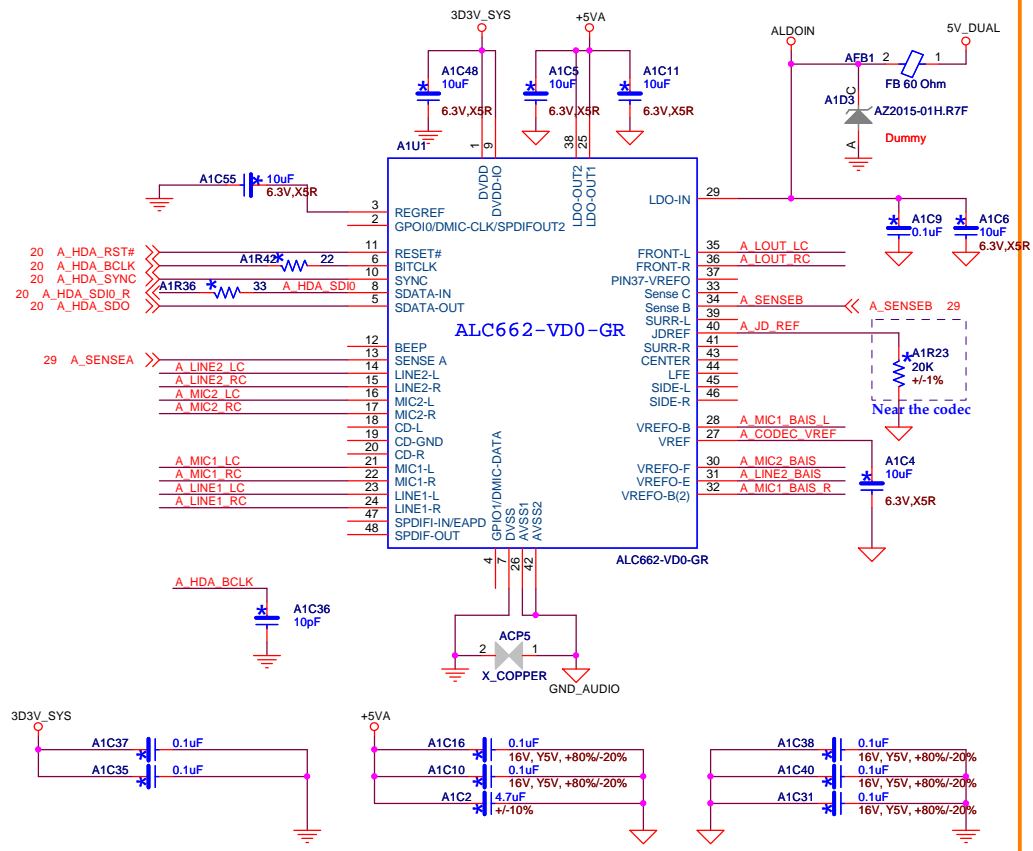
**FOXCONN®**  
**FOXCONN PCEG**

Title <b>DVI</b>		
Size C	Document Number <b>H61M06</b>	Rev A
Date: Thursday, January 05, 2012	Sheet 26	of 45

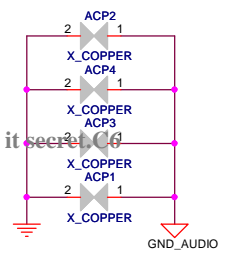
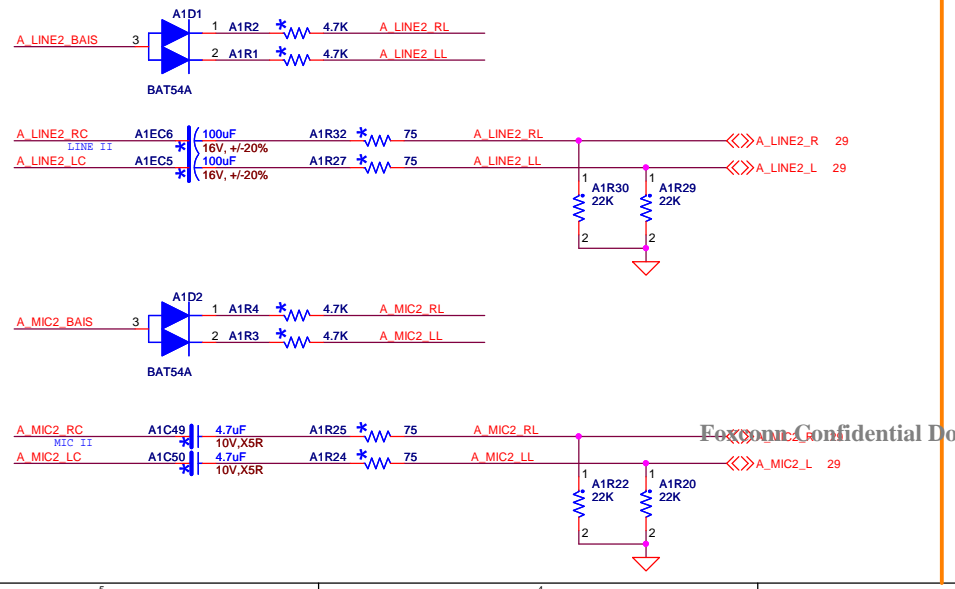


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<b>FOXCONN®</b>		
<b>FOXCONN PCEG</b>		
Title <b>PCIE 1X</b>		
Size C	Document Number <b>H61M06</b>	Rev A
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FRONT PANEL

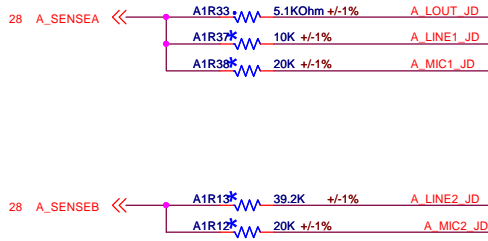


**FOXCONN**  
FOXCONN PCEG

Title <b>AUDIO-1:ALC889</b>		
Size A3	Document Number <b>H61M06</b>	Rev A
Date: Thursday, January 05, 2012	Sheet 28	of 45

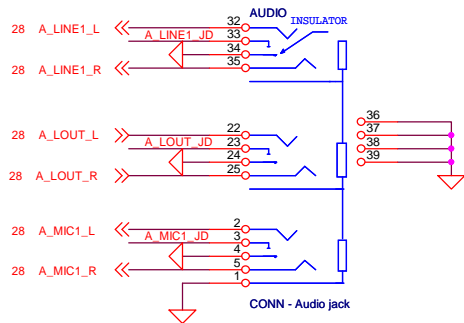
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### JACK SENSE



### +5VA for AUDIO

### Audio Jack



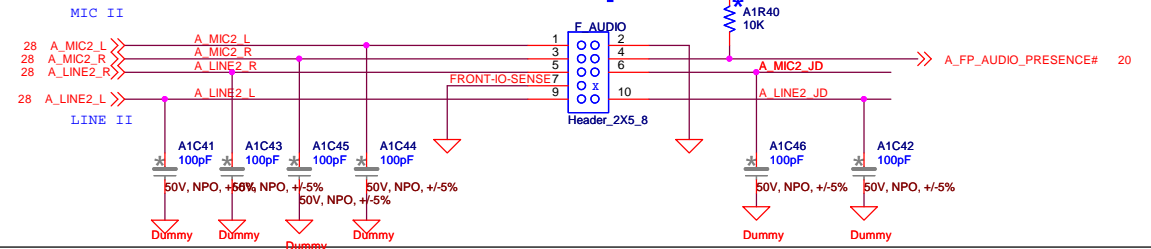
### Audio Jack

- LINE IN (UAJ)
- LINE OUT (UAJ)
- MIC IN (UAJ)

### Front\_Audio

FAB:1.0

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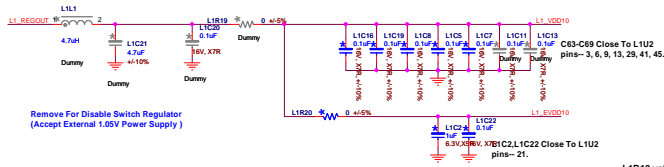
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**FOXCONN**<sup>®</sup>

**FOXCONN PCEG**

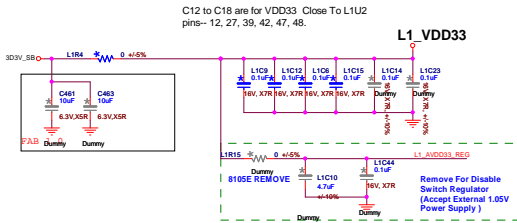
Title		<b>AUDIO-2:CONNECTOR</b>	
Size	Document Number	<b>H61M06</b>	
A3			Rev A
Date:	Thursday, January 05, 2012	Sheet	29 of 45

	1.05V / 1.0V source	L1L1	L1C21	L1C20	L1R8/ reserve	L1R11/ reserve
8111E Series/8111F Series/8105E Series	SWR	○	○	○	○	X
8105E Series (except for VL)	LDO	X	X	X	X	○
8111E Series/8111F Series/8105E-VB	External	X	X	X	X	○
8105E Series (except for VB)	External	X	X	X	○	X



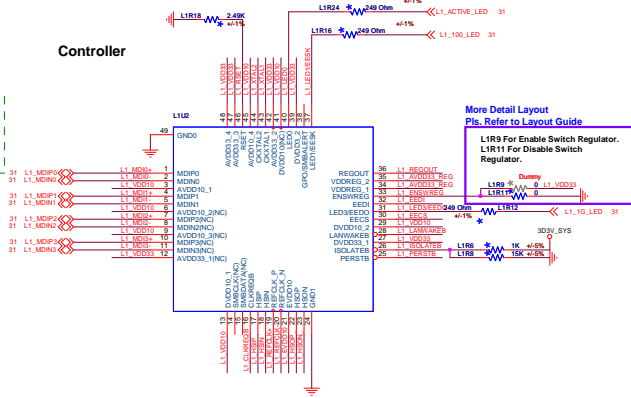
Remove For Disable Power Regulator (Accept External 1.05V Power Supply)

L1R18 value should be 2.49k (1%) for all application. LED define change after remove EEPROM

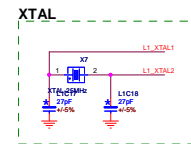


Remove For Disable Switch Regulator (Accept External 1.05V Power Supply)

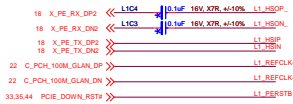
Controller



More Detail Layout Pls. Refer to Layout Guide  
L1R9 For Enable Switch Regulator.  
L1R11 For Disable Switch Regulator.



L1R26 0 Dummy 2SM\_CLK\_GEN 22



L1\_VDD33  
10K ohm close to Host side

L1R10 0 LAN\_WAKER L1\_LANWAKEB

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FOXCONN PCEG

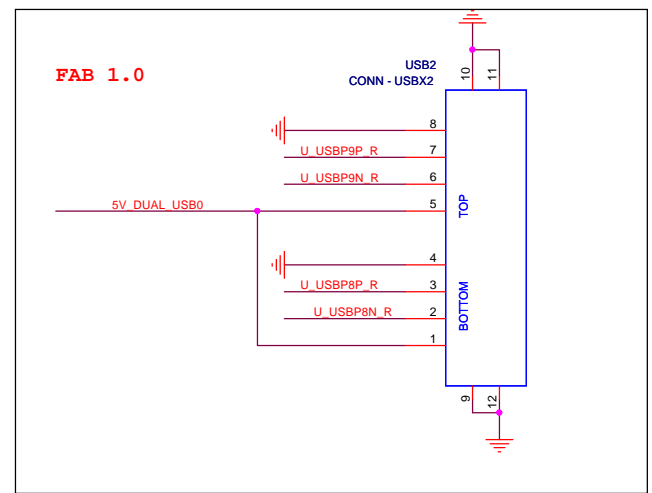
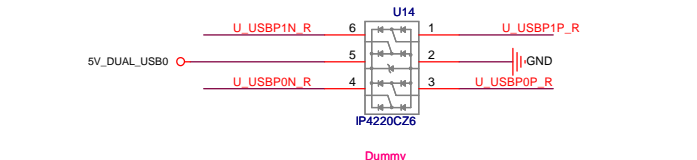
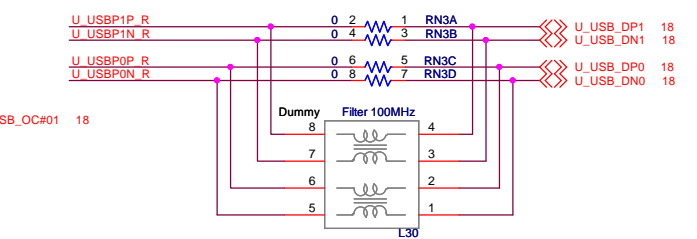
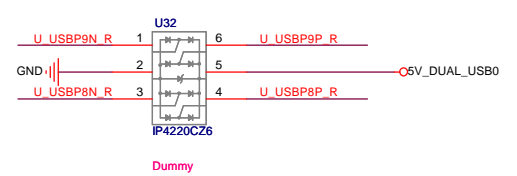
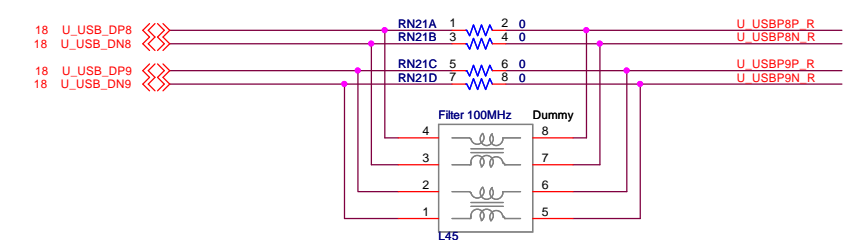
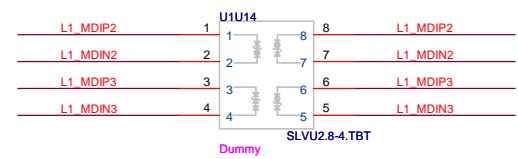
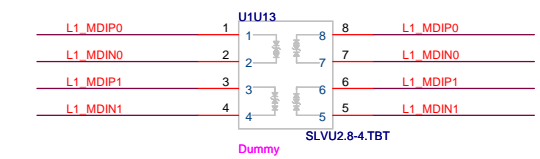
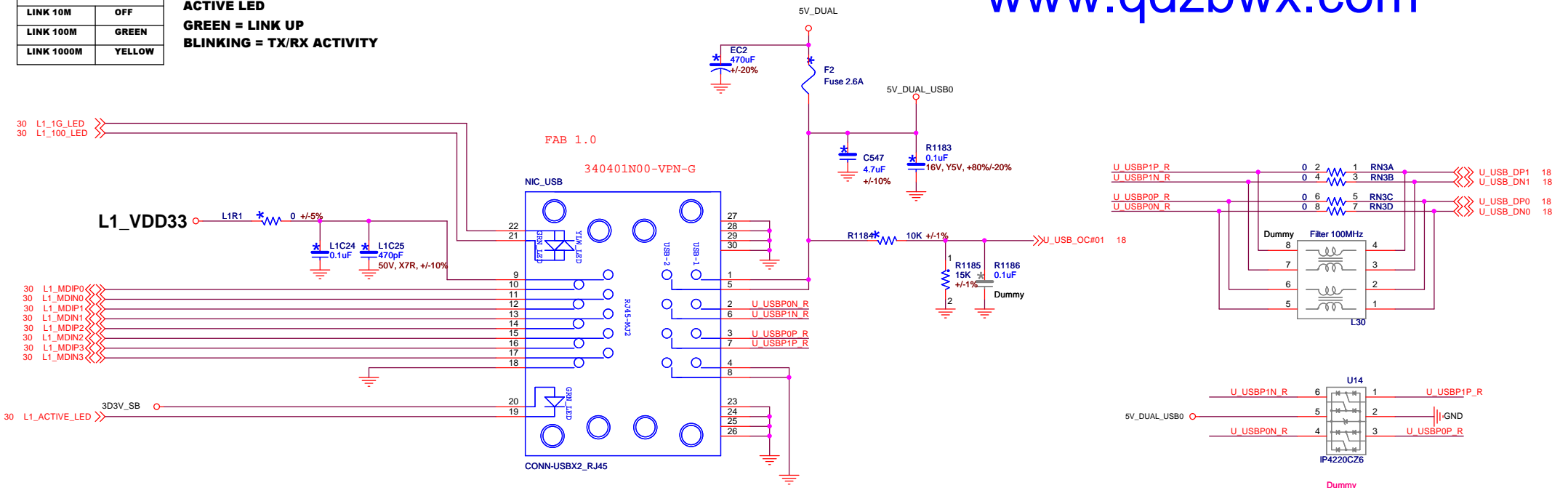
LAN

Document Number: **H61M06**

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SPEED LED	
LINK 10M	OFF
LINK 100M	GREEN
LINK 1000M	YELLOW

**ACTIVE LED**  
**GREEN = LINK UP**  
**BLINKING = TX/RX ACTIVITY**

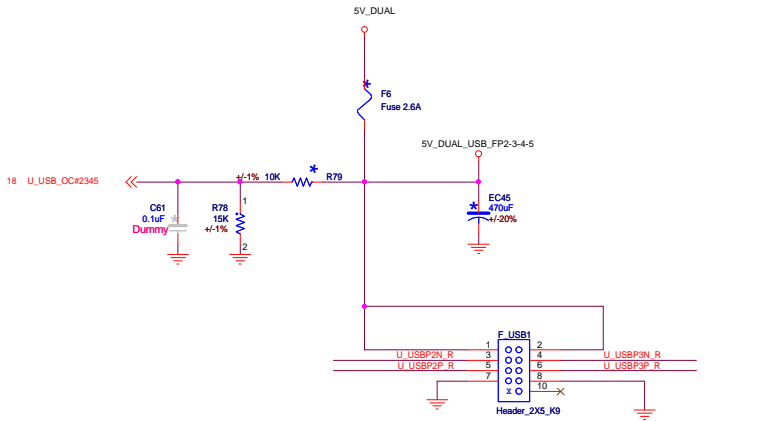


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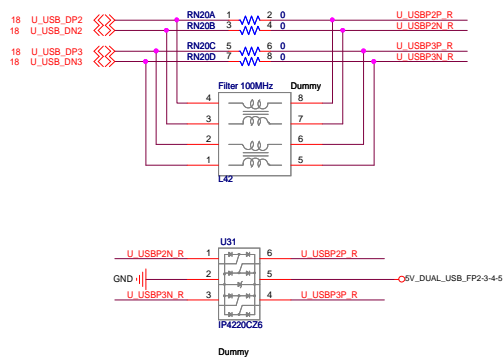
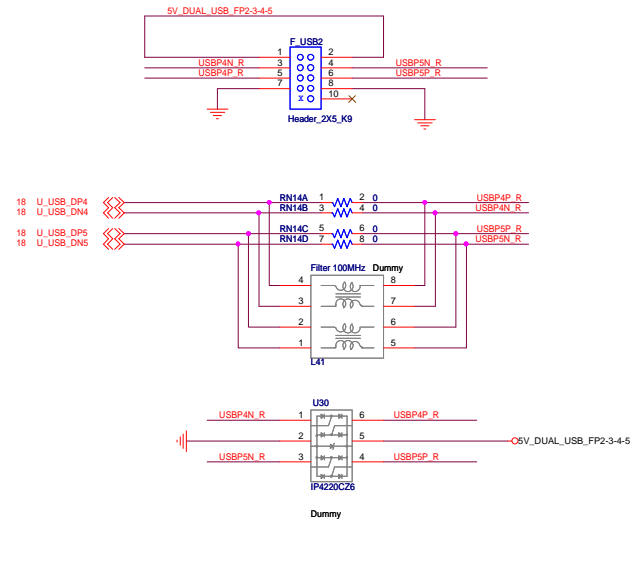
**FOXCONN**  
**FOXCONN PCEG**

Title: **LAN1/ USB Connectors**  
 Size: A3 Document Number: **H61M06**  
 Date: Thursday, January 05, 2012 Sheet 31 of 45

Front\_USB1



Front\_USB2



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**FOXCONN®**  
**FOXCONN PCEG**

Title: **Front USB2.0 Header**

Size C Document Number: **H61M06** Rev A

Date: Thursday, January 05, 2012 Sheet 32 of 45

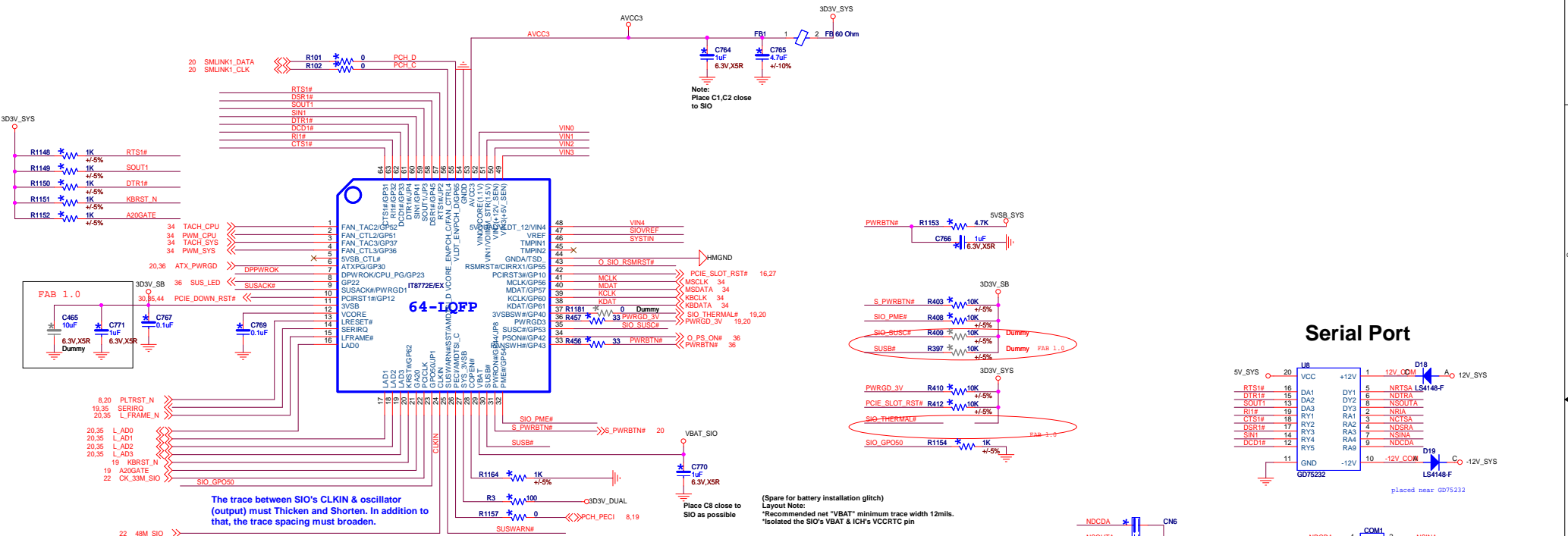


Power-On Strapping

JP1	Symbol	Value	Description
Pin-23	DSW_EUP_SEL	1	RIP (default)
JP2	WDT_EN	0	Disable WDT to reset PWROK(default)
Pin-57	FAN_CTL_SEL	0	Enable WDT to reset PWROK
JP3	FAN_CTL_SEL	1	EC Index 6bh/73h default = 80h
Pin-59	FAN_CTL_SEL	0	EC Index 6bh/73h default = 00h
JP4	K8PWR_EN	1	Disable K8 Power Sequence(default)
Pin-61	K8PWR_EN	0	Enable K8 Power Sequence

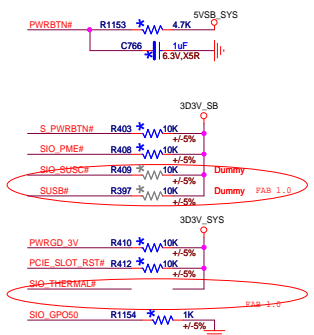
If without use these pins, Please pull-up. Don't let it floating

- 1.Pin 6:ATXPG
- 2.Pin 30:SUSB#
- 3.Pin Pin 23 / Pin 57/ Pin 59/ Pin61
- 4.Pin38-41 KCLK/KDAT/MCLK/MDAT
- 5.Pin 63 pull high to 3VSB

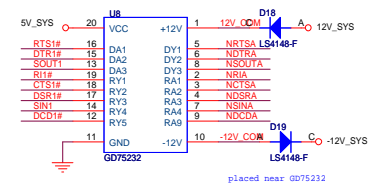


The trace between SIO's CLKIN & oscillator (output) must Thicken and Shorten. In addition to that, the trace spacing must broaden.

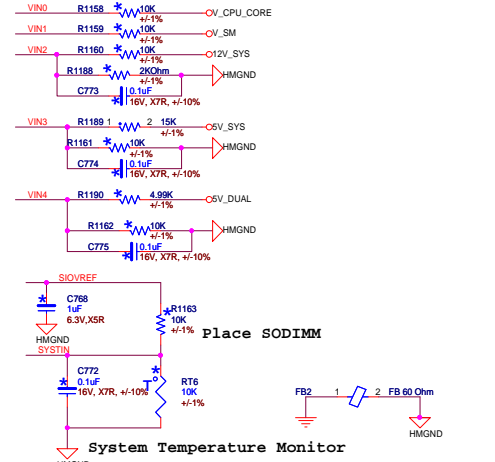
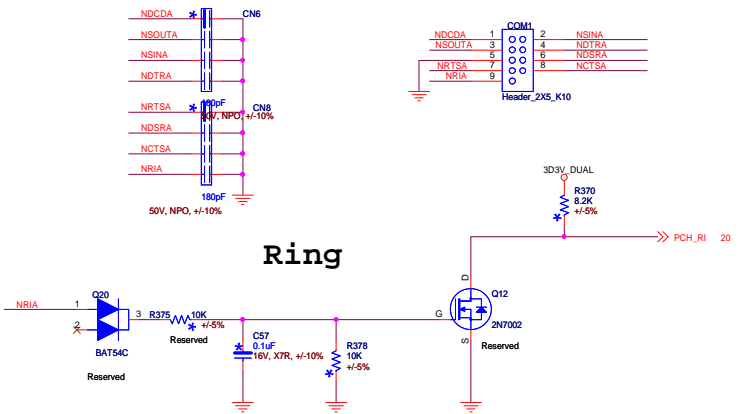
(Spare for battery installation glitch)  
Layout Note:  
"Recommended net "VBAT" minimum trace width 12mil.  
"Isolated the SIO's VBAT & ICH's VCCRTC pin



Serial Port



Ring



Place SODIMM

System Temperature Monitor

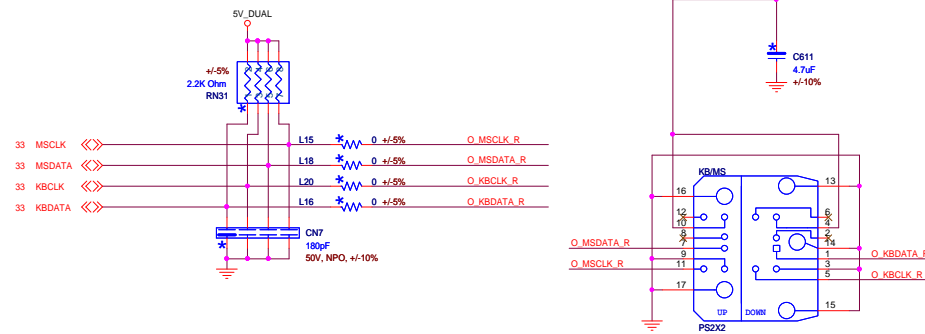
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Title		Super I/O IT8772	
Size	Document Number	H61M06	
C			
Date:	Thursday, January 05, 2012	Sheet	33 of 45

Add for EMI on 0929

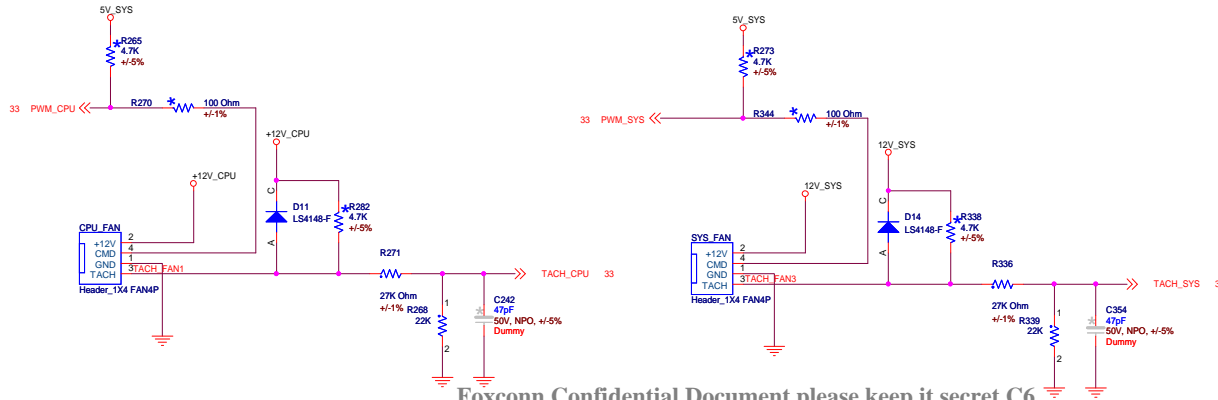
KB /USB connect



CPU FAN

SYS FAN

New FAN Header Definition  
pin1. GND  
pin2. +12V  
pin3. Sense  
pin4. PWM

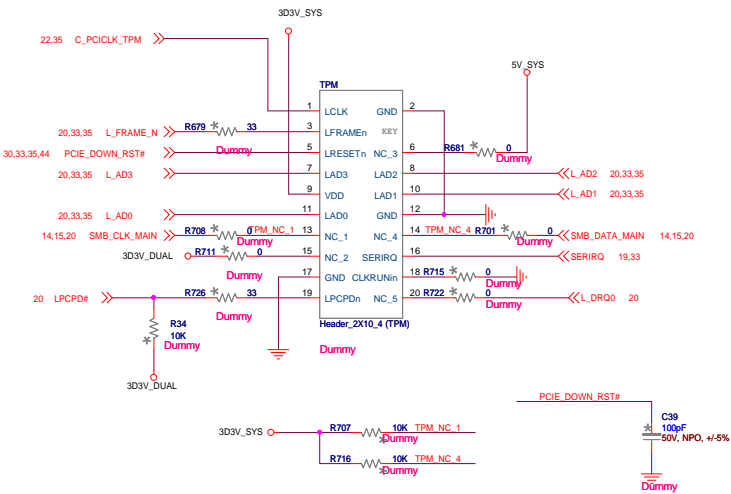


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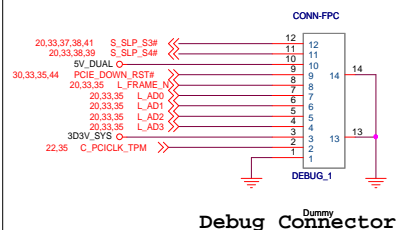
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Size: C  
Document Number: H61M06  
Date: Thursday, January 05, 2012  
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# TPM



# LPT PORT

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Debug Connector

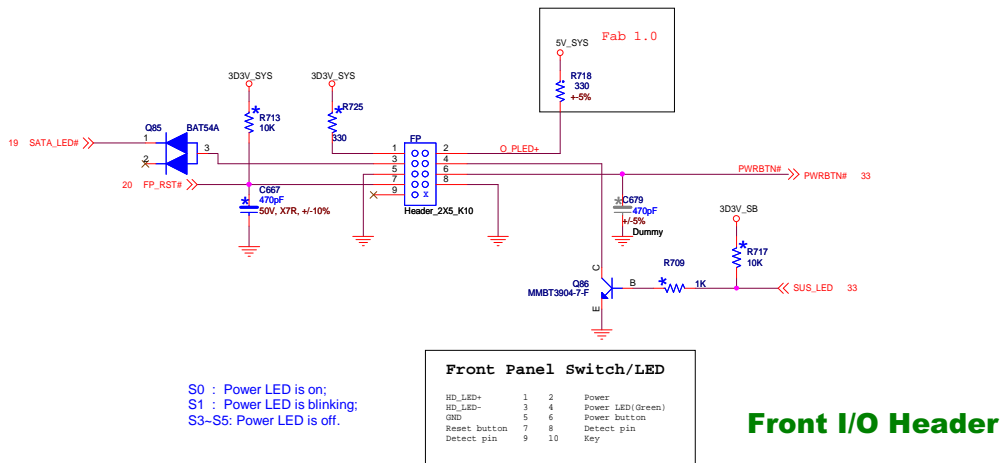
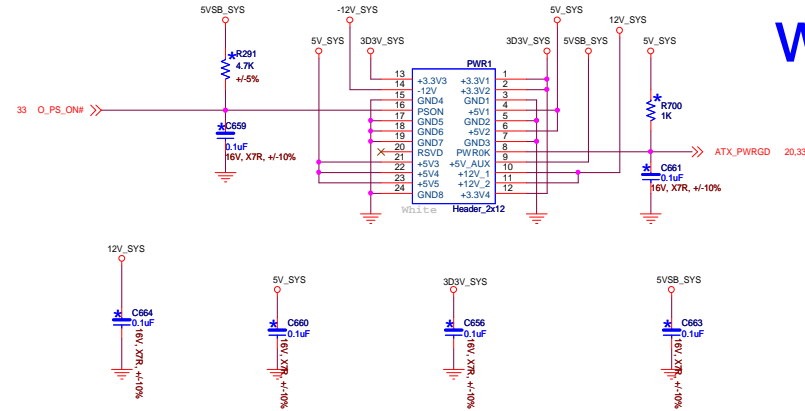
# COM HEADER

# COM PORT

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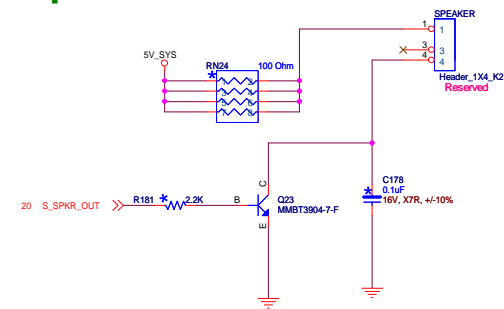
<b>FOXCONN®</b>		
<b>FOXCONN PCEG</b>		
Title <b>TPM/LPT/COM</b>		
Size C	Document Number <b>H61M06</b>	Rev A
Date: Thursday, January 05, 2012 Sheet 35 of 45		

# ATX POWER CONNECTOR

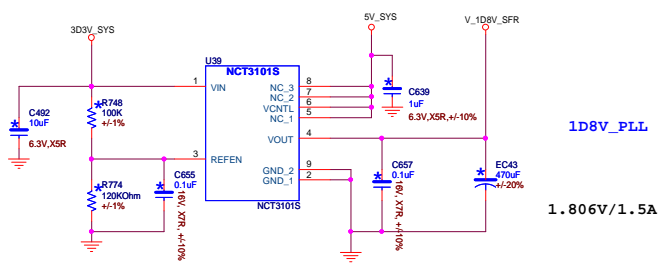
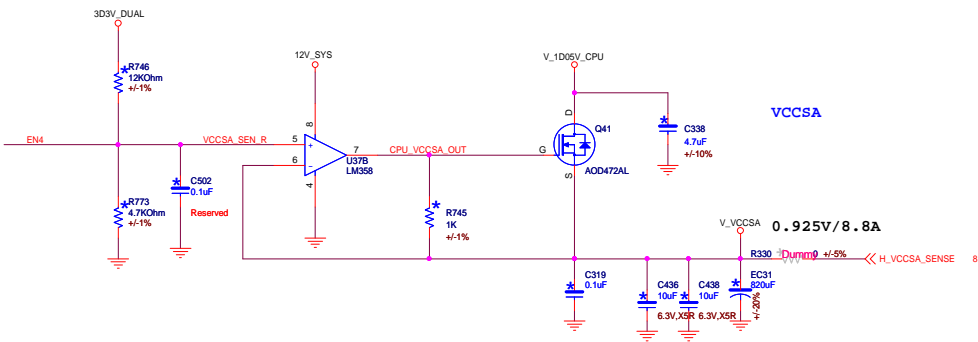
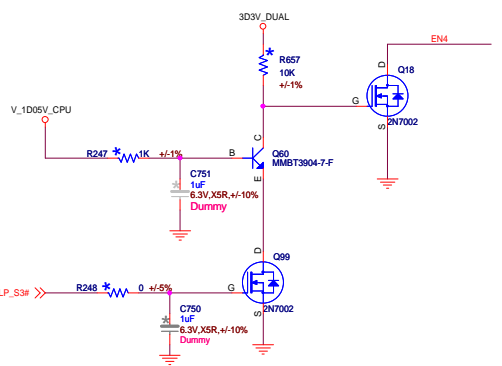
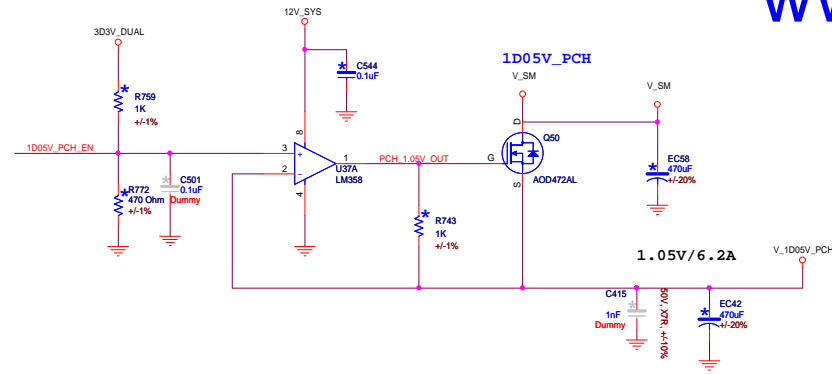
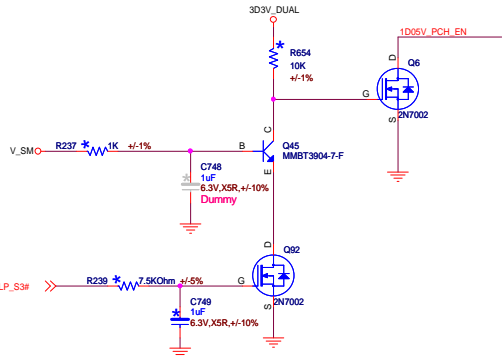


## Front I/O Header

## BUZZER/Speaker Header



Pull lo for 0.9V vref out and address 54h

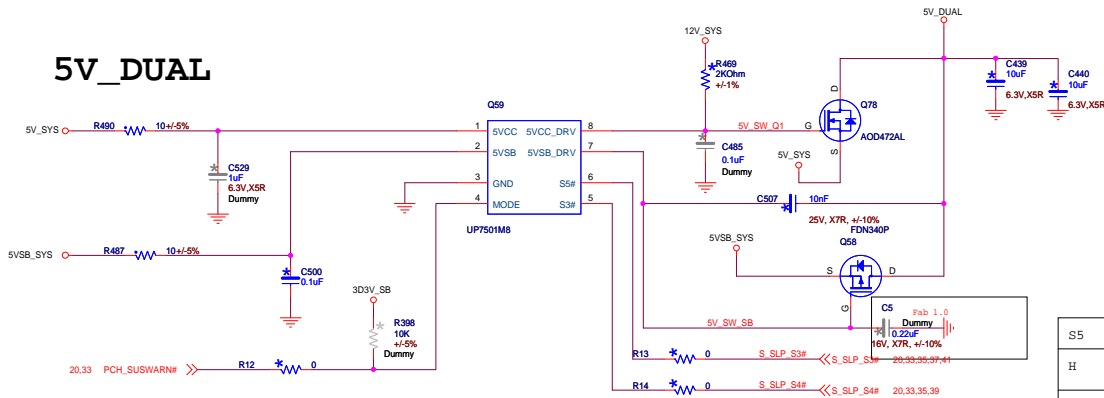


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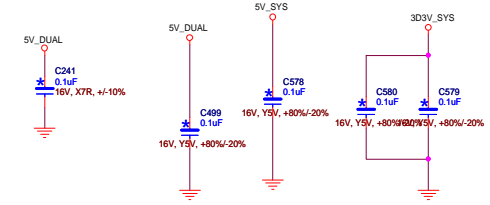
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 Size C: Document Number H61M06 Rev A  
 Date: Thursday, January 05, 2012 Sheet 37 of 45

### 5V\_DUAL

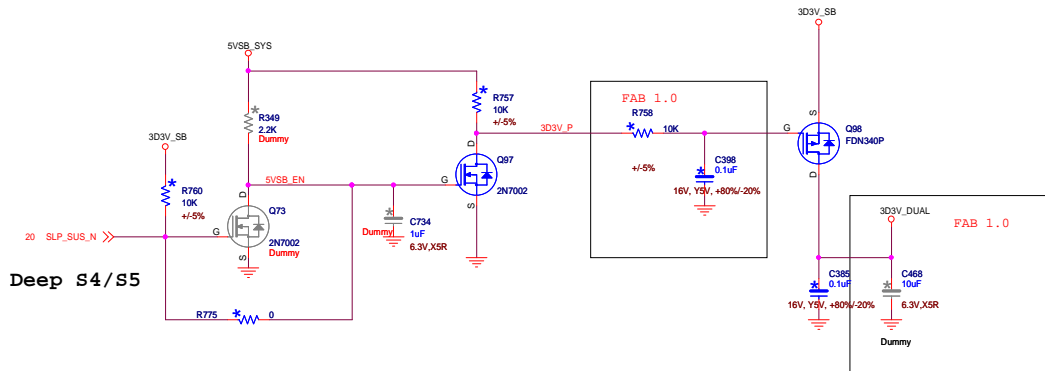


HI= S4/S5 5VDUAL FORM 5VSB  
Low= S4/S5 5VDUAL TURN OFF

S5	S3	NODE	5VDUAL
H	H	X	5VCC
H	L	X	5VSB
L	X	H	5VSB
L	X	L	Shutdown

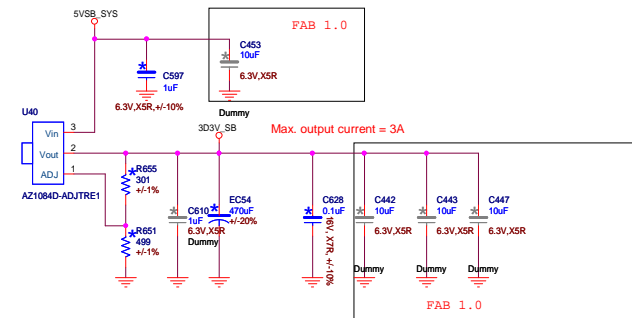


### 3D3V\_DUAL



Deep S4/S5

### 3D3V\_SB



$V_{out} = V_{ref} (1 + R2/R1) + I_{adj} R2$   
 R1 is Up Resistor.  
 $I_{adj} = 50\mu A$   
 $V_{ref} = 1.25V$

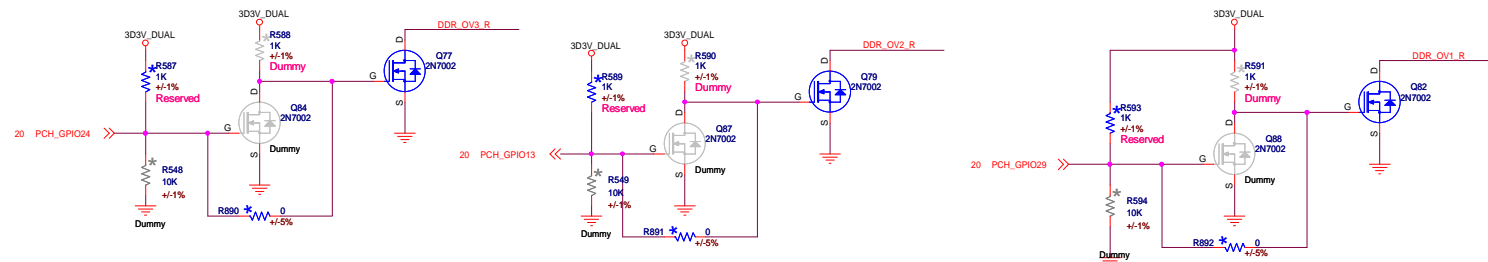
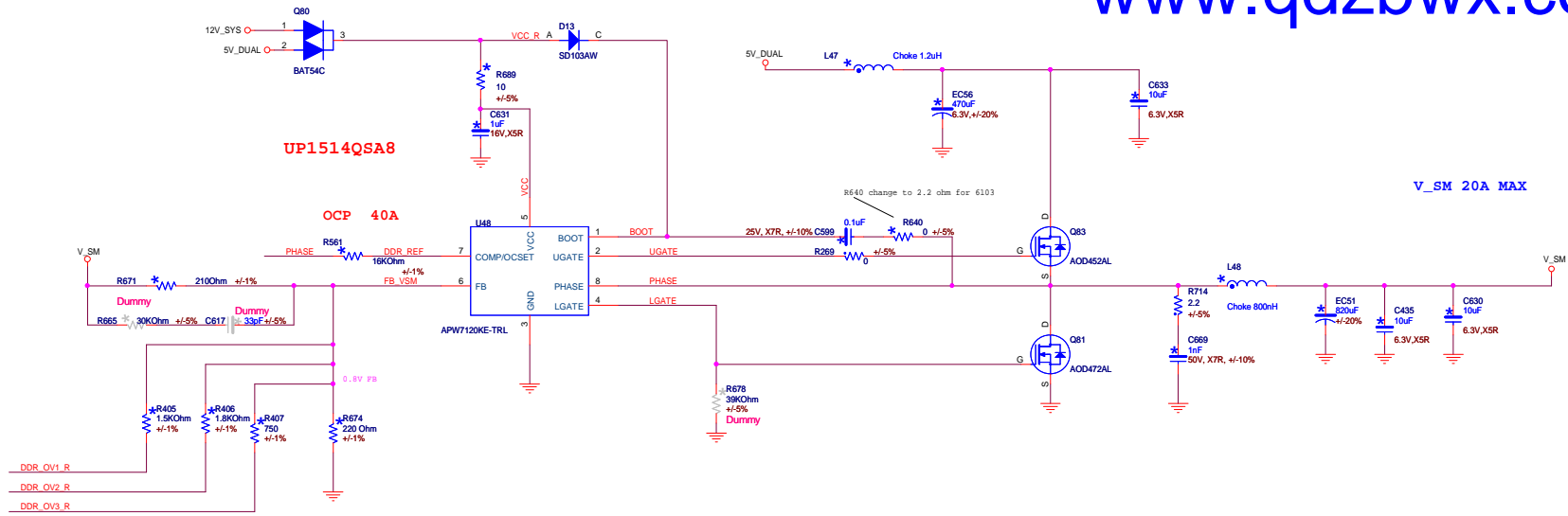
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Title: 5V\_DUAL/3.3V\_SB/3.3V\_DUAL

Size: Document Number H61M06 Rev A

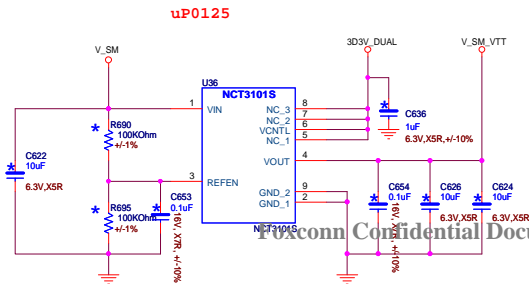
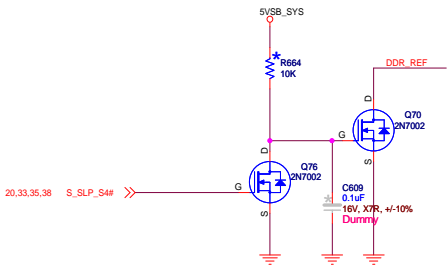
Date: Thursday, January 05, 2012 Sheet 38 of 45



**DDR POWER**  
DDR Voltage

Max=40A  
27A in design guide

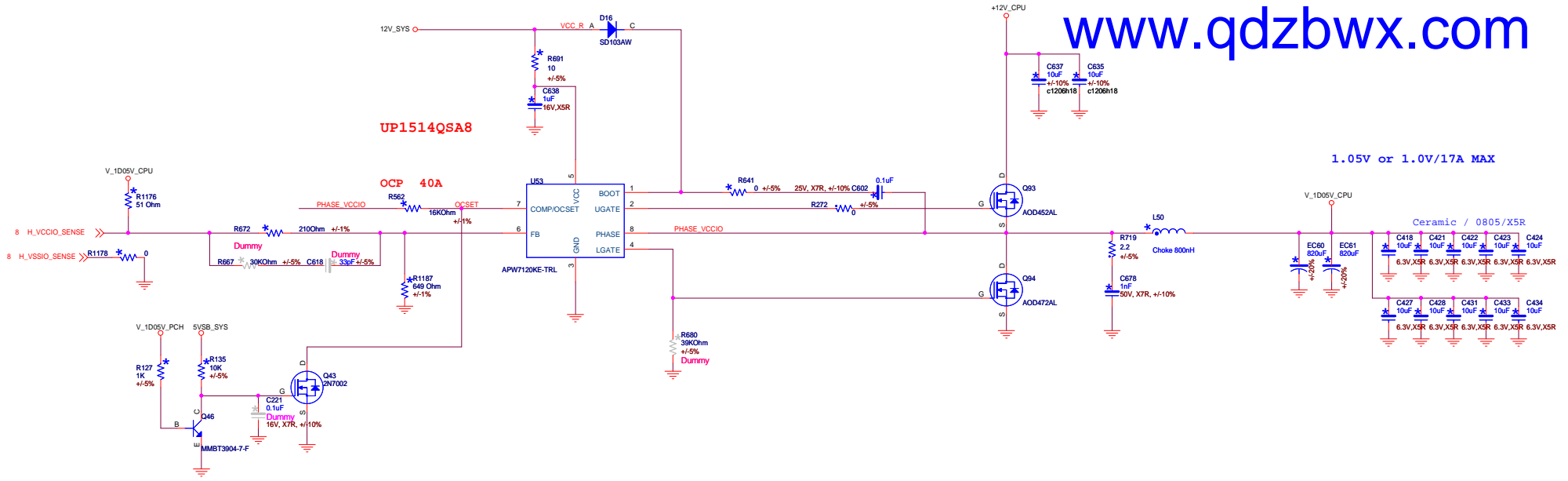
GPIO24	GPIO13	GPIO29	Voltage
0	0	0	1.563636364
0	0	1	1.675636364
0	1	0	1.656969697
0	1	1	1.768969697
1	0	0	1.787636364
1	0	1	1.899636364
1	1	0	1.880969697
1	1	1	1.992969697



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Title: 1D5V\_STR  
 Size C: Document Number H61M06 Rev A  
 Date: Thursday, January 05, 2012 Sheet 39 of 45



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FOXCONN PCEG

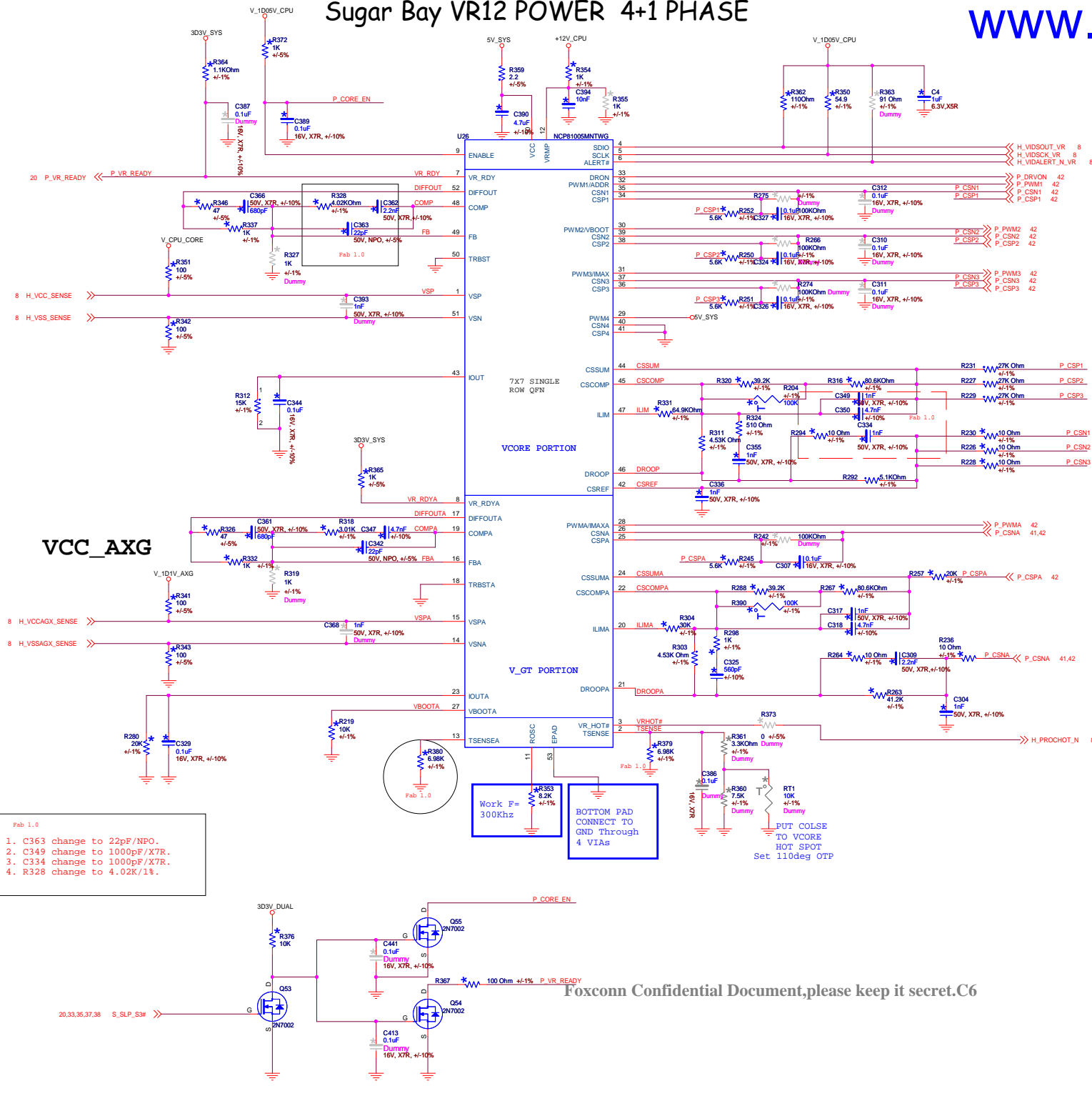
Title: CPU\_VCCIO

Size: C Document Number: H61M06 Rev: A

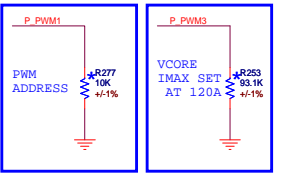
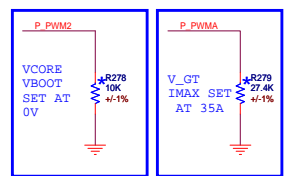
Date: Thursday, January 05, 2012 Sheet: 40 of 45



# Sugar Bay VR12 POWER 4+1 PHASE



## VCC\_CORE



## BOOT VOLTAGE

RESISTOR VALUE	BOOT VOLTAGE
10K	0V
25K	0.9V
45K	1.0V
70K	1.1V
95K	1.2V
125K	1.35V
165K	1.5V

## PWM ADDRESS

RESISTOR VALUE	SVID ADDRESS FOR VCORE RAIL	SVID ADDRESS FOR V_GT RAIL
10K	0000	0001
25K	0010	0011
45K	0100	0101
70K	0110	0111
95K	1000	1001
125K	1010	1011
165K	1100	1101

- Fab 1.0
1. C363 change to 22pF/NPO.
  2. C349 change to 1000pF/X7R.
  3. C334 change to 1000pF/X7R.
  4. R328 change to 4.02K/1%.

Work F = 300KHz

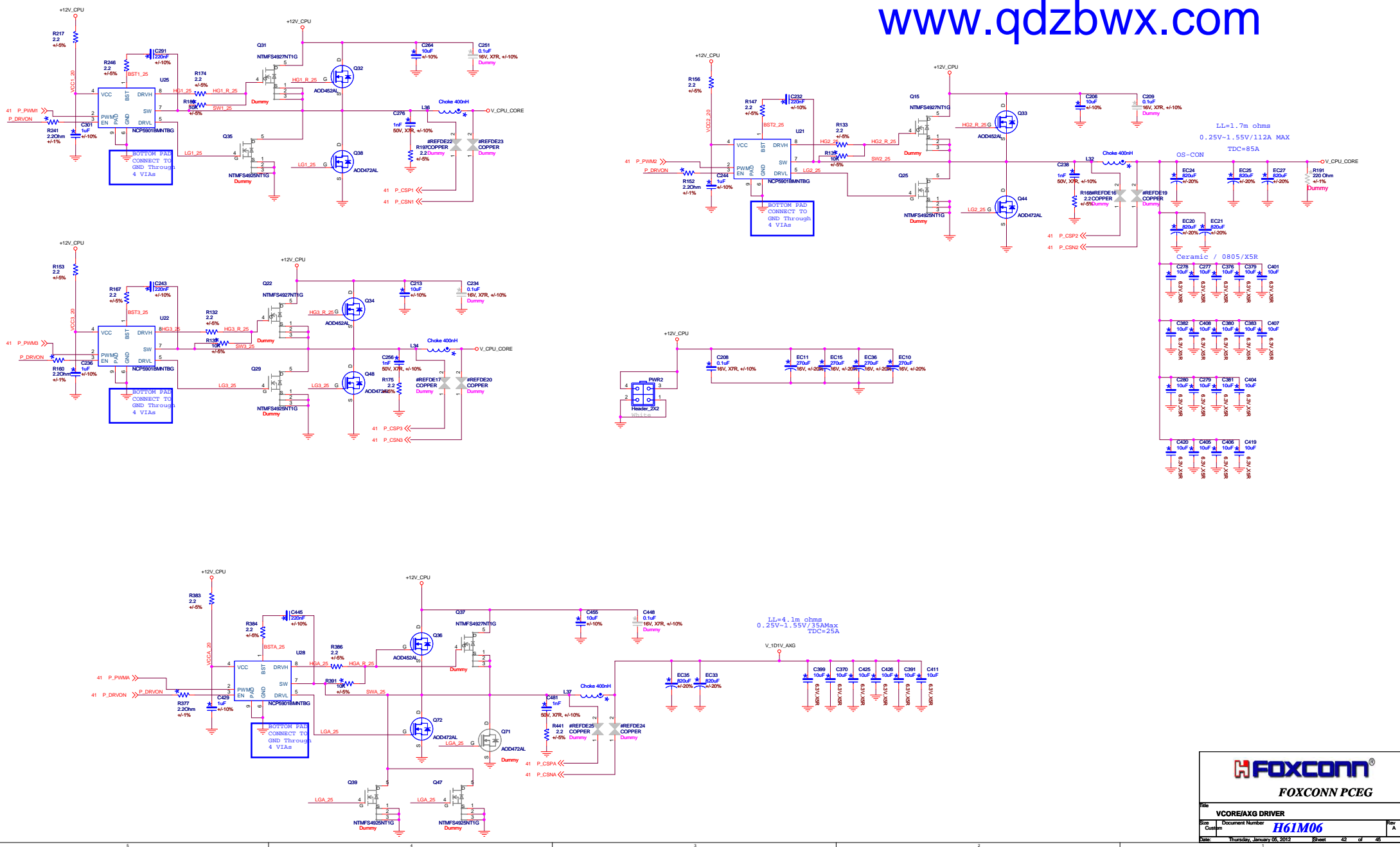
BOTTOM PAD CONNECT TO GND THROUGH 4 VIAS

PUT COLSE TO VCORE HOT SPOT Set 110deg OTP

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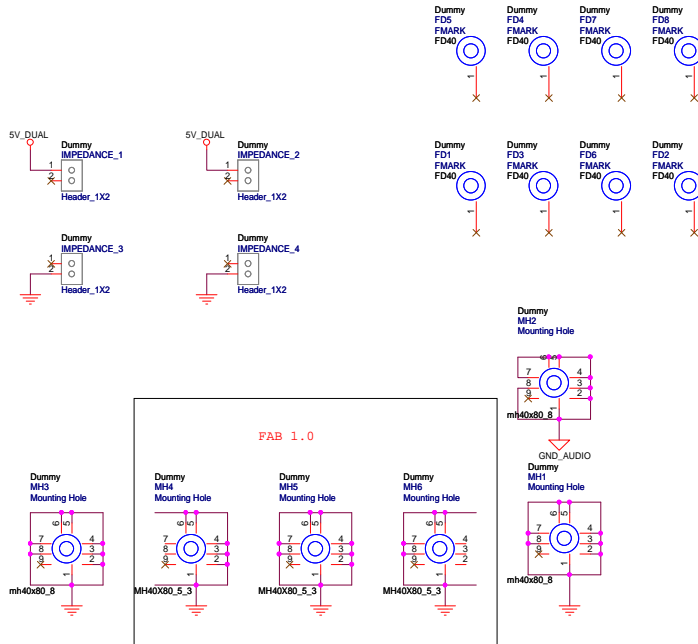
**FOXCONN**  
FOXCONN PCEG

Title: VCORE/AXG PWM  
Size: C Document Number: H61M06  
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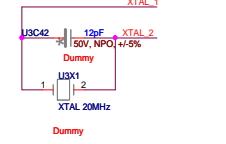
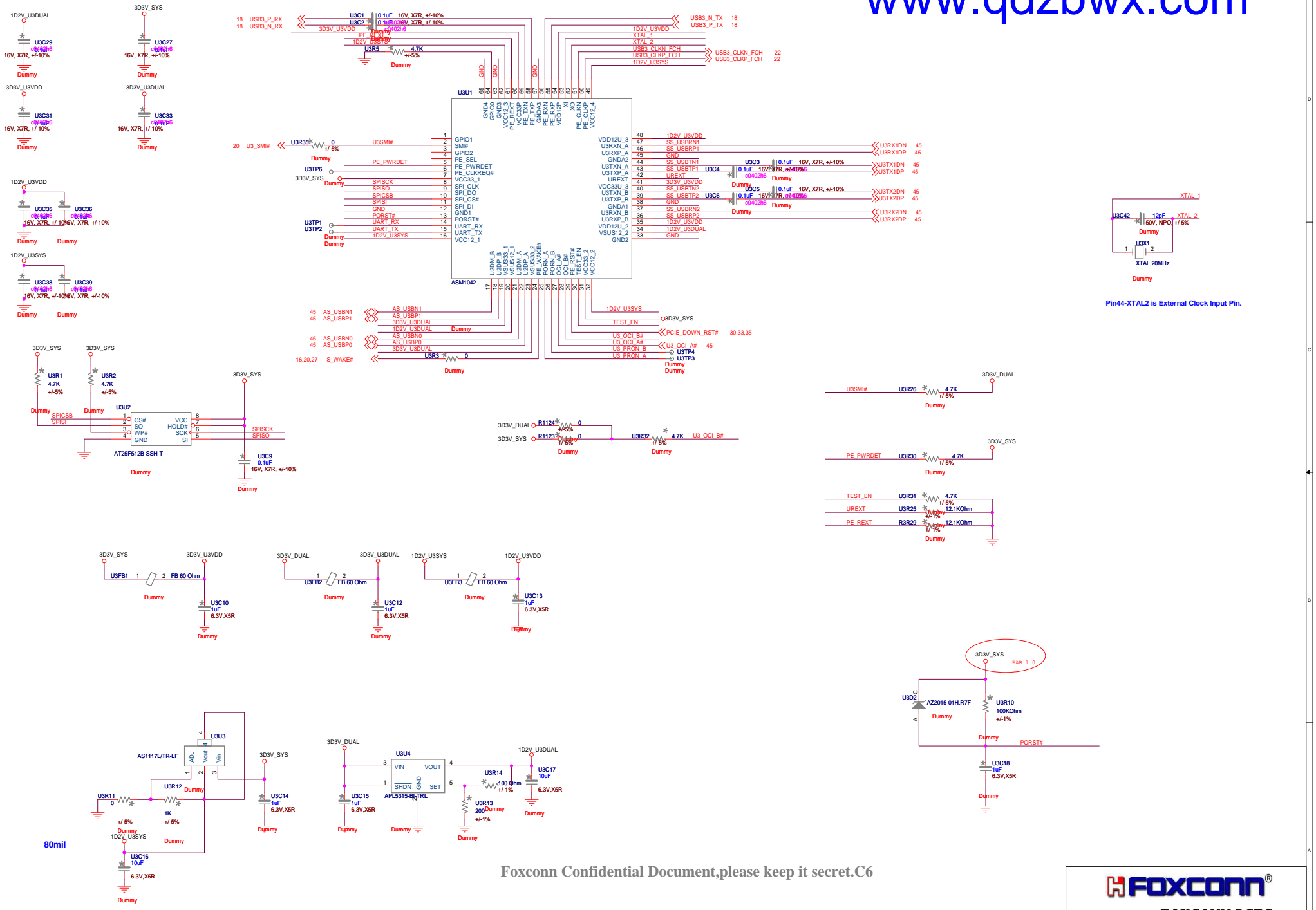
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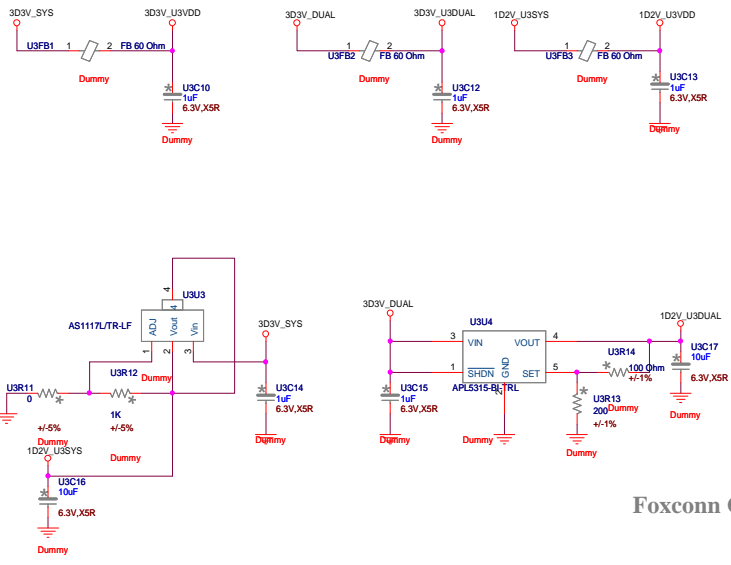
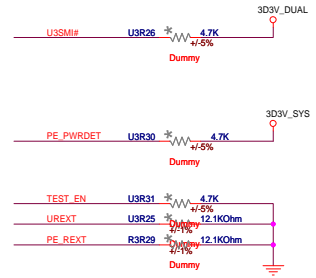


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<b>THROUGH HOLE</b>		
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Pin44-XTAL2 is External Clock Input Pin.



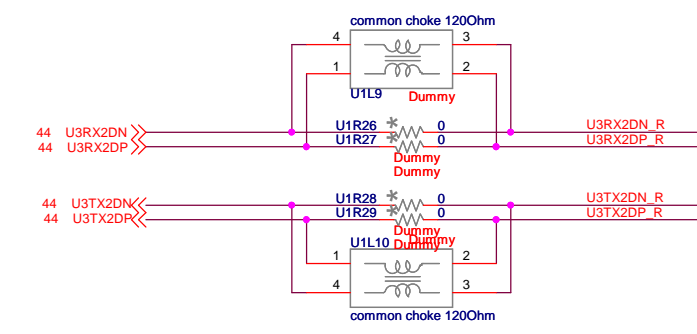
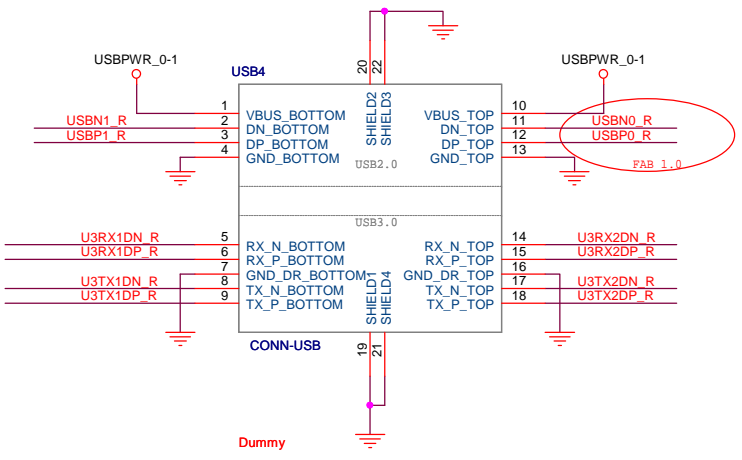
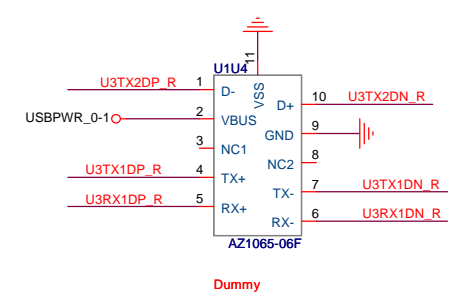
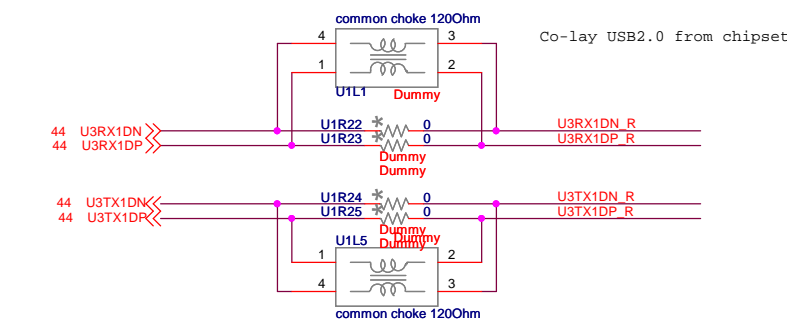
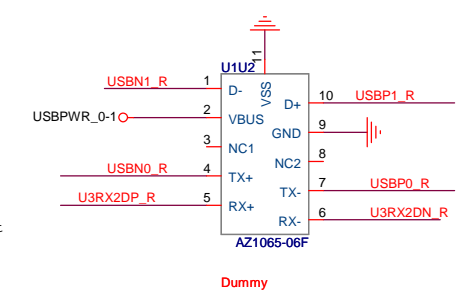
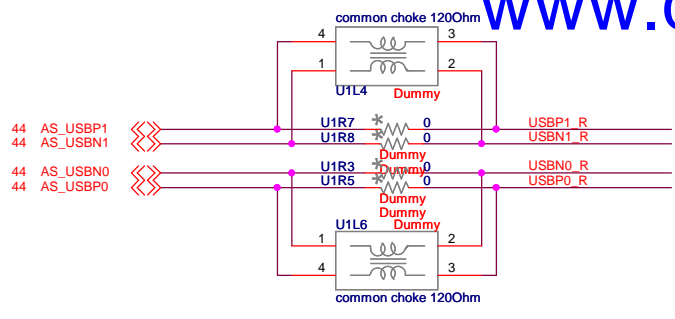
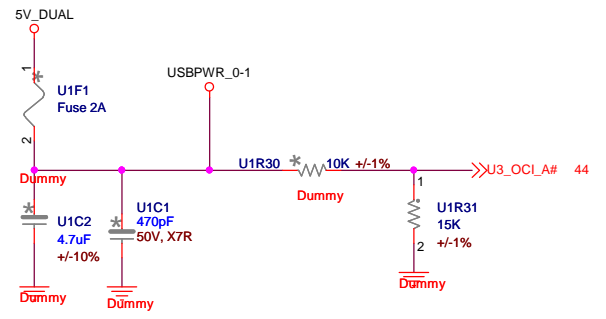
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FOXCONN PCEG

Title: **USB3**

Size: C Document Number: **H61M06** Rev: A

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